Extensible 2×N Quantum Dot Arrays: Encoding Arrays of Spin Qubits Implemented Using Holes in a Germanium Heterostructure

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A thesis presented for the degree of
Master's of Physics, MSc.

UNIVERSITY OF COPENHAGEN
FACULTY OF SCIENCE

Abstract

Quantum computing[1] has long promised to revolutionise all the natural sciences, and thereby the world at large. The ability to perform calculations at speeds far beyond the capabilities of classical computers has the potential to solve problems that are currently intractable[2]. The field of quantum computing has seen rapid development in recent years, with many different platforms being developed and tested. One of the platforms that has garnered interest, is the spin qubit[3]. Spin qubits are a promising platform for quantum computing as they have conquered most of the DiVinzenco criteria[4], except for one: scalability. This thesis presents the development of a theoretically scalable platform, presents simulations[5] pertaining to the efficacy of the designs, and discusses the fabrication and measurements of the devices.

The platform is based on a germanium heterostructure[6,7], which has been demonstrated as an excellent platform to host hole spin qubits[8]. The design is based on a $2\times N$ array of quantum dots, which recent research has shown could be the route to a fault-tolerant error corrected platform[9]. Our results show that these designs can be automated by parametric design schemes, increasing the speed by which the designs can be modulated. We demonstrate stable and convergent simulations of the parametric designs via an open-source implementation of the Poisson equation, which is done to ensure that the design performs as intended. The designs are then fabricated and measured. While the fabrication process needs to be optimised to improve the quality of the devices, these are promising early results. Measurements of the devices show that the devices are functional, but the quality of the devices is not yet at a level where quantum operations can be performed.

By providing these results, we lay the groundwork for extendable $2\times N$ arrays of quantum dots.

Acknowledgements

Firstly, I would like to thank **Anasua Chatterjee** for her guidance and support throughout the project as my advisor. She will be greatly missed here in Copenhagen, but Delft has gained a wonderful professor.
While **Ferdinand Kuemmeth** was not directly involved as an advisor to this project, he has still provided thoughtful and insightful feedback on the project, and for that, I thank him greatly.

I owe a great amount of gratitude to both **William Ian Leonard Lawrie** and **Lazar Lakic** for their combined guidance and support throughout the project. Their knowledge and expertise have been invaluable to me, not to mention their daily shenanigans and friendly demeanor which makes QDev a wonderful place to work.

While fabrication is a fun endeavour in and of itself, it would not have been nearly as much fun without the assistance and company of - **Charalampos "Harry" Lampadaris**, **Casper Wied**, **Arnulf Johannes Snedker-Nielsen**, and **Harold Lim Co**.

A great thank you to the Spin Qubit Group at NBI - **Anton Zubchenko**, **Rune Kutchinsky**, **Marcin Kepa**, **Tsung-Lin Chung**, **Torbjørn Rasmussen**, **Bertram Brovang**, **Fabrizio Berritta**, **Jürgen Luus**, **Johanna Malina Zeis**, and **Fabio Ansaloni**. I have enjoyed working with you all and have learned a great deal from each of you.

QDev as a centre would not be functional without its staff, and for that, I thank you - **Lena R. Jacobsen**, **Ingrid Vernimmen**, **Smitha Nair Themadath**, **Nader Payami**, **Katrin Hjort**, **Martin Bjergfelt**, **Zhe Liu**, **Subhadip Das**, and **Maria João Batista**.

I would also like to extend a thanks to all the other QDev colleagues that I have worked with during my time here. You've all been wonderful coworkers - **Daniel Fogh**, **Rasmus Dalsgaard Schlosser**, **Joachim Elbeshausen Sestoft**, **Vasileios Vlachodimitropoulos**, **Malthe Asmus Marciniak Nielsen**, **Ksenia Shagalov**, **Rune Thinggaard Hansen**, **David Feldstein Bofill**, **Zhenhai Sun**, **Michaela Eichinger**, **Johann Bock Severin**, **Chaoyue Wang**, **Amalie Terese Jiao Paulsen**, **Shikhar Sing**, **Federico Poggiali**, **Serwan Asaad**, **Gunjan Piyush Nagda**.

I thank **Sebastian Utecth** for his assistance in perpetual coffee drinking and non-stop banter.

If I have forgotten anyone, please consider yourself included!

I would like to thank my parents, **Palle Liebe** and **Jette Liebe** for their continued support and encouragement throughout my studies. I would not have been able to complete this project without their support. Thank you, **Mathias Liebe**, for being a great brother.

Finally, I dedicate this thesis to my partner, **Caitlyn Jeanette Liebe**, for her unwavering support and love throughout my studies. We've always been there for eachother, and we will continue for many years to come.

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1.

Introduction

In the past four decades, scientists from the natural sciences, have worked on the development of a quantum computer. While significant progress has been made, many different implementations compete for superiority. The quantum computer is a fundamentally different machine than the classical computer, and as such, the physical platform on which it is built, must be fundamentally different. One of the main challenges still facing the field, is the scalability of the physical platform, as the quantum computer must be able to perform calculations on a large number of qubits, in order to solve problems that are intractable for classical computers.

This work aims to explore the challenges associated with proposing an extensible quantum computer based on isolated spins in a semiconductor platform, in a comprehensive manner.

The initial steps to realising such a quantum processor are rooted in the design and structure of a device, which must be physically stable, addressable, and scalable. These challenges are adressed in Section 2.

Once an initial design has been proposed, it is particularly helpful to simulate the device, in order to predict its behaviour, and to optimise its performance, especially when working with non-trivially produced materials, as is the case in this work. Work on this can be found in Section 3.

Following the realisation of a workable simulation, the next step is to fabricate the device, and to characterise its properties. This is adressed in Section 4.

Finally, the device must be tested, measured, and its performance must be evaluated. Experimental set-up and results of this can be found in Section 5.

Before going into the specifics of this work, it is beneficial to explore introductory concepts of quantum information, the physical implementation criteria, and the spin qubit, which is adressed in Section 1.1 and Section 1.2.

1.1 Introductory Quantum Information

The quantum bit (qubit) draws its name from the bit used in conventional computer science. The bit, or the binary digit, can be either 0 or 1. This informational basis unit is the foundation of all traditional computing, most implemented as a transistor. A qubit, in the same way, is the informational basis of quantum computing, and it can be represented by any two-level quantum mechanical system. The qubit state can be represented using a general superposition of the basis vectors $|0\rangle$ and $|1\rangle$[10,11] , which are also known as the computational basis states:

$$|\psi\rangle = \alpha|0\rangle + \beta|1\rangle \tag{1.1}$$

Equation (1.1) is the general superpostional state of a two-level quantum mechanical system. We require that[12,13] $\langle\psi \mid \psi\rangle = 1$, such that α and β are complex numbers, where $|\alpha|^2$ and $|\beta|^2$ are interpreted as the probability amplitude, i.e., the probability of observing that state given an experimental mea-

surement. From this interpretation it follows that: $|\alpha|^2 + |\beta^2| = 1$, which we can geometrically interpret as the norm of the state in vector space always being equal to 1.

This superposition can be exploited to generate algorithms that outperform their classical counterparts by up to exponential factors[14,15,16,17,18] and some have already been implemented experimentally[19,20,21,22]. Furthermore, by entangling qubits, one can encode large amounts of information in a small number of qubits[23].

1.1.1 A Qubit, The Bloch Sphere, and Quantum Gates

The probabilistic interpretation of the amplitudes, i.e., $|\alpha|^2 + |\beta|^2 = 1$, allows us to rewrite Equation (1.1) into

$$|\psi\rangle = e^{i\gamma}\left(\cos\left(\frac{\theta}{2}\right)|0\rangle + e^{i\varphi}\sin\left(\frac{\theta}{2}\right)|1\rangle\right), \tag{1.2}$$

where γ is denoted as the global phase, which *has no effect on the observable state*. This can be shown from the calculation of the expectation value of the state[12]: $|\psi|^2 = \langle\psi \mid \psi\rangle = \psi^*\psi$, in which the state and its conjugate are multiplied, cancelling any global phase. For this reason, it can be ignored, and the equation is rewritten:

$$|\psi\rangle = \cos\left(\frac{\theta}{2}\right)|0\rangle + e^{i\varphi}\sin\left(\frac{\theta}{2}\right)|1\rangle \tag{1.3}$$

The angles θ and φ denote a point on the unit sphere, which is denoted as the *Bloch sphere*[10], and can be seen on Figure 1. It is a representation of the state space, which a qubit inhabits. The states $|0\rangle$ and $|1\rangle$ represent the computational basis for quantum algorithms, and are located at the poles of the Bloch sphere. It is a useful tool in visualising how one can interact with the qubit. The operations performed on qubits, such as switching between state $|0\rangle$ and $|1\rangle$, can be visualised as rotations around the x-, y-, and z-axes. As the Block sphere is a visualisation of the single-qubit system, we can define a set of operations on the qubit as rotations around the three axes of the Bloch sphere. We define X_θ, Y_θ, and Z_θ[10,23,24] as rotation around the x-, y-, and z-axes of degree θ, respectively.

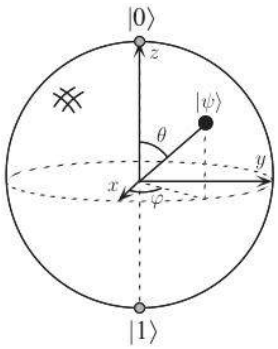

Figure 1

The Bloch Sphere: State space of a qubit or any two-level quantum mechanical system.[23]

$$X_\theta = \begin{pmatrix} \cos\left(\frac{\theta}{2}\right) & -i\sin\left(\frac{\theta}{2}\right) \\ -i\sin\left(\frac{\theta}{2}\right) & \cos\left(\frac{\theta}{2}\right) \end{pmatrix}, Y_\theta = \begin{pmatrix} \cos\left(\frac{\theta}{2}\right) & -\sin\left(\frac{\theta}{2}\right) \\ \sin\left(\frac{\theta}{2}\right) & \cos\left(\frac{\theta}{2}\right) \end{pmatrix}, Z_\theta = \begin{pmatrix} e^{-i\frac{\theta}{2}} & -i\sin\left(\frac{\theta}{2}\right) \\ -i\sin\left(\frac{\theta}{2}\right) & \cos\left(\frac{\theta}{2}\right) \end{pmatrix} \tag{1.4}$$

Setting $\theta = \pi$, we recover the Pauli operators:

$$X_\pi = \sigma_x = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix} \tag{1.5}$$

$$Y_\pi = \sigma_y = \begin{pmatrix} 0 & i \\ -i & 0 \end{pmatrix} \tag{1.6}$$

$$Z_\pi = \sigma_z = \begin{pmatrix} 1 & 0 \\ 0 & -1 \end{pmatrix} \tag{1.7}$$

To allow for the creation of superpositional states, we set $\theta = \frac{\pi}{2}$.
To achieve what is known as a universal gate set, as is mentioned in the following section, we also need a two-qubit entangling gate, such as the Controlled-Not (CNOT), Controlled-Z (CZ) or SWAP[24,25]. At this point, it becomes beneficial to introduce the concept of the target and control qubit. The target qubit is the qubit which is affected by the conditional demand on the control qubit. For the CNOT gate, if the control qubit is in state 1, then a σ_x operation is performed on the target qubit. If not, no operations are performed. The functionality of the CZ gate is identical, but with a σ_z operation performed instead of the σ_x gate.

1.2 Physical Implementations

The hardware with which to build a quantum computer is still a heavily researched field, and all the physical platforms that have been proposed up to the present date have their distinct advantages and disadvantages. A qualitative benchmark and comparison of the platforms can be made using the five DiVincenzo criteria[4]

1. **Scalability**: A physical system which posseses a well-defined qubit, and which can be scaled to larger sizes. The scalability is a key feature of quantum computers, for a couple of reasons: Firstly, it is necessary to be able to perform computations on a large number of qubits, in order to be able to solve problems that are intractable for classical computers. Secondly, due to imperfect conditions and operations, it is necessary to be able to perform error correction, which requires a large number of qubits to be able to encode a single logical qubit.
2. **Initialisation**: One must be able to initialise the system into a well-known state, such as $|0\rangle$. If one cannot initialise the system into a known state, it is impossible to perform any meaningful calculation on it.
3. **Long Coherence Times**: Such that the system can maintain its state for a long time. If the system cannot maintain its state for sufficient times to perform both gates and read-out of the system, then one cannot perform calculations on it. As a reference time-scale, these are typically on the order of micro- to milliseconds.
4. **Universal Gate Set**: The system must be able to perform any unitary operation on the qubits. To perform calculations with the qubits, one must be able perform gates on them. If one cannot perform all rotations one single qubits, and an appropriate conditional two-qubit operations, then all functional quantum algorithms are out of reach. This universal gate set is usually a single two-qubit operation, and three single-qubit rotational operations, from which all other operations can compiled.
5. **Measurement Capability**: the system can be measured in the computational basis. The measurement of the system, before the system reaches incoherent states due to noise and undesired couplings, is key to performing any algorithm.

Over the last few decades, most of these criteria have been well-adressed in various physical platforms, such as ion traps[26,27,28] , superconducting circuits[29,30,31] , photons[32,33,34] , semi-conductors[35,18,3,36] , et cetera[37]. Most have been met. However, the issue of scalability remains a challenge. The inherent difficulty in maintaining coherence and operating on quantum objects, due to the high susceptibility to noise, difficulty in trapping individual quantum objects, and the challenge of adressing them both individually and to couple them has imposes numerous constraints on the scalability of various systems.

1.2.1 Isolated Spins as a Qubit Platform

The binary, superpositional nature of the spin of a (quasi-) particle, makes for a natural qubit candidate, as it is a fundamentally quantum mechanical feature, and as such, a general spin is described by Equation (1.1).

There a few caveats to the spin-qubit platform, which have to do with the nature of the spin. The physical platform needs to be able to address the spins individually, and as a part of a larger two-qubit gate. One of the crucial elements of the addressability is the time-scale, as the spin is coupled to its surroundings, and will therefore have spin-relaxation mechanics[38] that can originate from spin-orbit coupling, exchange interactions, and hyperfine interactions with nuclear spins, amongst others. Spin relaxation is the phenomemon in which a qubit relaxes into a lower, energitically favourable state. The time-scale of the spin relaxation, designated as T_1, must be longer than the time-scale of the intential interaction and read-out.

Another limitation is the dephasing time, which is the time-scale on which the qubit maintains its phase coherence. The phase coherence is most often destroyed by the qubit being coupled to its surroundings, such as a spin-orbit coupling or a coupling to a surrounding spin-bath[39]. The dephasing time is quantified by the time-scale T_2, and it is upper bounded by T_1 as the relaxation of the spin also induces loss of phase information.

The semi-conductor platform has emerged as a promising candidate for the sub-field of spin qubits. Specifically germanium[24,6,40] has garnered attention due to low effective masses, which relaxes the fabrication requirements of the quantum dots, the high spin-orbit coupling, which enables purely electronic manipulation of the spins[41], and the availability of nuclear spin-depleted, isotopically purified ^{70}Ge, which promotes an Overhauser gradient free environment for the charge carriers. However, one of the most important factors, is that the platform is compatible with the existing semi-conductor industry and its foundries. This compatability enables a successful germanium based spin qubit platform to exploit the successes of the existing industry, to alleviate the fabricational and scalability issues of other approaches.

Even with the advantages of the semi-conductor platform, the fabricational requirements are no easy feat. The quantum dots must be fabricated with high precision, and the spins must be addressable both individually and as a part of a larger system. The scalability of the system is a particular challenge, as the spins must have controlled interaction with each other, and the system must be able to perform calculations on a large number of qubits.

In this work, we focus on the Loss-DiVincenzo qubit system[42], in which a single spin acts as the two-level system. Other systems exists, where it is not the individual spin that acts as a qubit, but a combination, such as the singlet-triplet two spin system, or the exchange-only two-spin system. A singlet-triplet and an exchange-only system could also be viable in this specific platform, and in the design proposed in Section 2.5.2

2.

The Physical Platform and Parametric Design

The physical platform the qubits are realised in, is an important aspect of the quantum processor. The platform must be able to confine and manipulate the qubits, in such a manner that provides high fidelity[43], and long coherence times, in addition to providing the means for read-out of the qubit state. The platform must also be scalable, such that a large number of qubits can be realised. In this work, we focus on the use of quantum dots as the confinement and manipulatory measure, of a two-dimensional hole gas (2-DHG) in a germanium/silicon-germanium heterostructure. We also use a parametric design approach to create the physical platform, which allows for trivial modification of the design, and easy scaling of the design to a large number of quantum dots.

2.1 Quantum Dots

A quantum dot[11,44,45,46,47] is an electrically operated set of gate electrodes, which provide confinement of particles in a semi-conductor platform. By employing both static and dynamic electromagnetic fields, one can engineer platforms in which a quantum well can either accumulate or deplete into a single-particle regime in the spatially localised electromagnetic fields. Accumulation mode is a scenario in which the quantum well is initially depleted of the particle of choice, and the electromagnetic fields are engineered such that we can accumulate particles into the 2D quantum well. In this work, we focus on accumulation-mode germanium based 2-dimensional hole gasses.

2.2 Coulomb Phenomena, Charge Sensing, and Radio-Frequency Reflectrometry

There are several phenomena that are crucial to the operation of a quantum dot, such as the concepts of Coulomb blockade, Coulomb oscillations, charge sensing, and radio-frequency reflectrometry. These phenomena allow for the manipulation and read-out of the qubit state. In this section, we will go through these phenomena, and explain how they are used in the operation of a quantum dot.

2.2.1 Coulomb Blockade and Coulomb Oscillations

For the 2-DHG to be able to accumulate charge carriers, there needs to a be resevoir to draw from, to load charges into the quantum well. The resevoir is a charge-carrier sea, which is assumed to be practically infinite, for all intents and purposes.

Such a charge-carrier sea coupled to the quantum dot is shown on Figure 2, **a** - **d**.

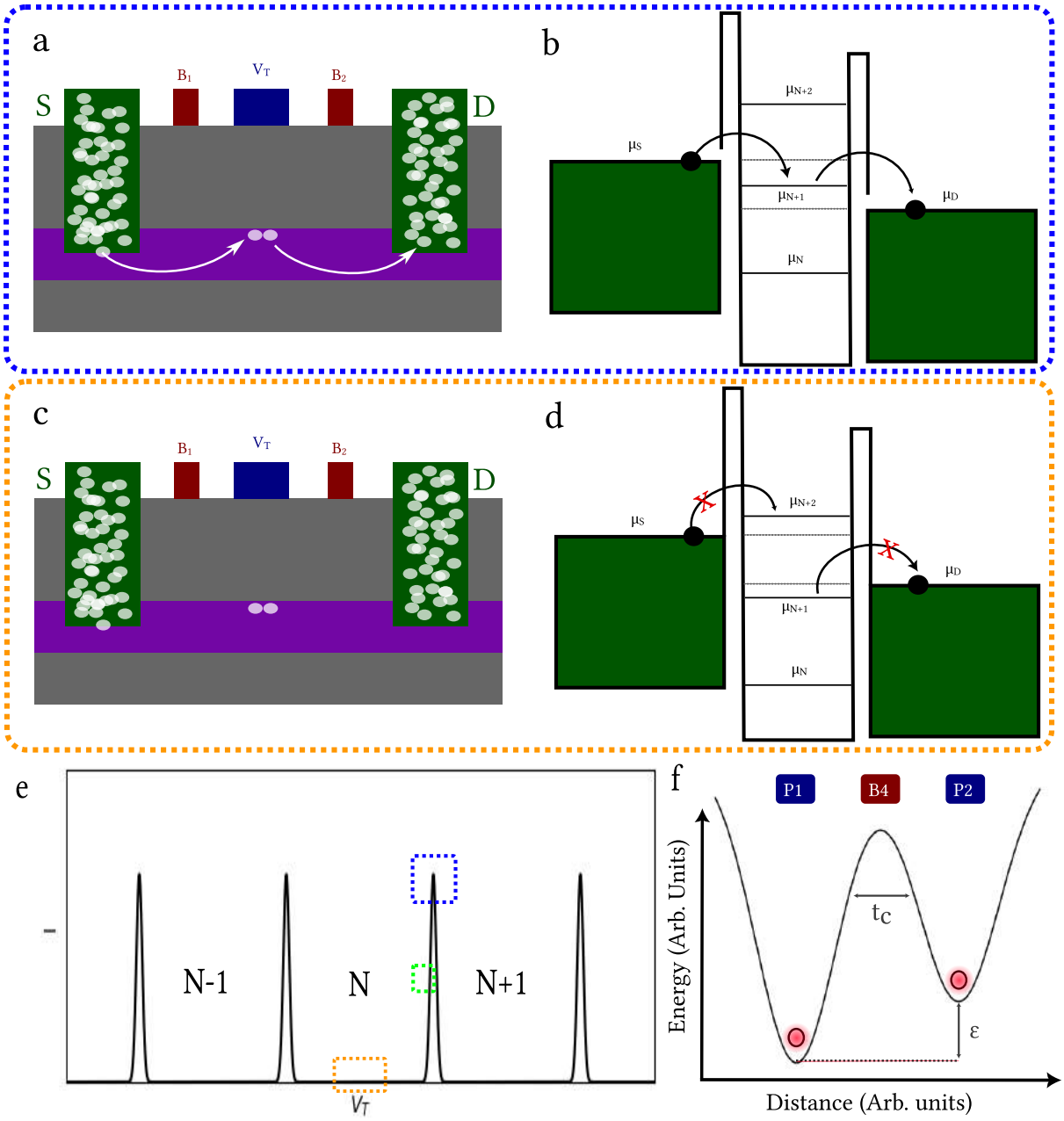

Figure 2 **a**: Current flowing through the quantum dot from the resevoir to the drain, due to an available state in the quantum well. **b**: An available state in the quantum dot allowing charges to flow through, from the biased source to the drain **c**: The state in the quantum well is not available for charge transport; it is in Coulomb blockade. **d**: The quantum dot is in the Coulomb blockade regime, where the state in the quantum well is not available for charge transport. **e**: Oscillations seen in the charge spectrum, due to a the quantom dot being in alternating states of Coulomb blockade and charge transport. V_T denotes the top gate voltage, and I is the current. Yellow outline: Coulomb blockade. Blue outline: Transport regime. Green outline: Charge Sensing Regime[48]. **f**: Two neighbouring quantum dots, where the tunnel coupling is designated as t_C and the detuning is designated as ε. Adapted from[24]

The source and drainapply a voltage bias, $V_{SD} = \alpha(\mu_S - \mu_D)$, where α is the lever-arm (a metric of how strongly a change in gate voltage corresponds to a change in chemical potential), i.e., their re-

spective chemical potentials change, such that $\mu_S > \mu_D$. This results in a current flowing from the resevoir to the drain, through the quantum dot. The binary criteria for current flow is: either the state in the quantum well is available for charge transport, or it is not. The criteria for transport is thus: $\mu_S > \mu_N > \mu_D$, where N is the N'th charge occuptation of the quantum dot. When the state is available, charges can flow through the quantum dot, and the quantum dot is said to be in the charge transport regime. When the state is not available, the quantum dot is said to be in the Coulomb blockade regime. The oscillations seen in the charge spectrum, are due to the quantum dot being in alternating states of Coulomb blockade and charge transport. This is a crucial feature of the quantum dot, as the incredibly sharp features of the Coulomb oscillations allow for the sensing of single charge changes in the quantum well, which is essential for the read-out of the qubit state.

2.2.2 Charge Sensing and Spin Readout

By taking advantage of the sharp features of the Coulomb oscillations, one can use the quantum dot as a charge sensor. Consider Figure 3, **a**, where a double quantum dot system is shown. Is is sectioned into two sub-systems: The sensor dot and the two quantum dots. The sensordot will have a capacitative coupling to both quantum dots, such that a change in the occupancy of either quantum dot will result in a change in the measured current through it. By parking the sensordot in the blue region of Figure 2, **e**, the sensordot is fully in the transport regime, and the current through it is maximised. When the occupancy of either quantum dot changes, the measured current will shift, towards the green region, due to a change in the chemical potential, μ_S, of the sensordot via the capacitative coupling.

This charge sensing is a crucial component in the building a quantum computer, as it allows for the fullfilment of DiVincenzo criteria no. 5: read-out of the qubit state via a principle known as spin-to-charge conversion, expounded on in the following section.

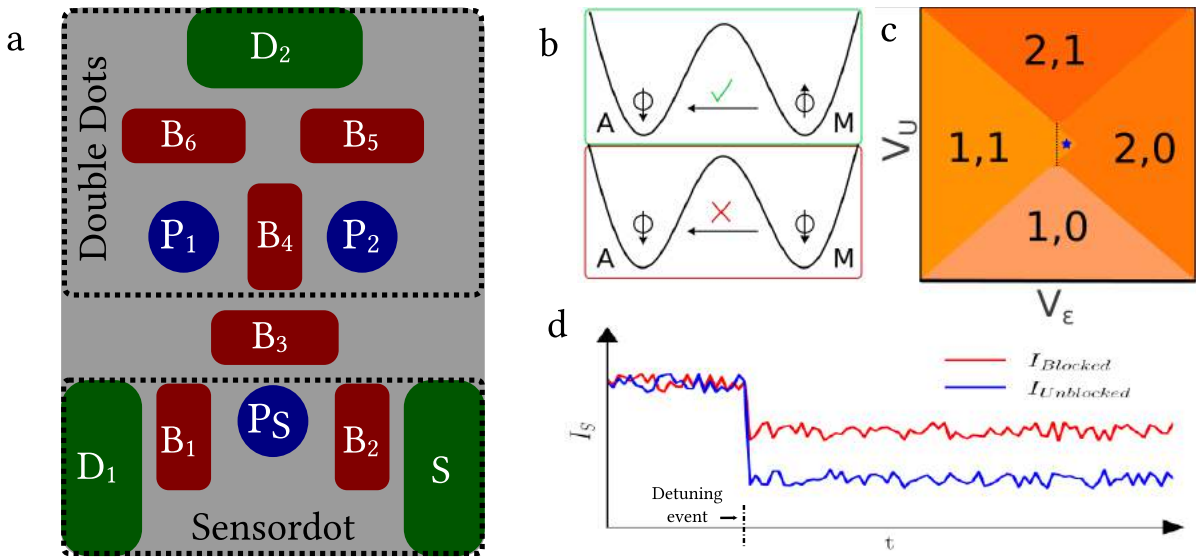

Figure 3 **a**: Sketch of a double quantum dot system. Alpha-codes: P for plunger, B for barrier, S for source, D for drain. **b**: Allowed tunneling and Pauli spin-blockade. **c** Charge stability diagram, where ε is the detuning between the dots, and V_U represents the eigenenergies of the charge occupation levels in the system. **d**: The spin-to-charge conversion current, where the current through the sensor dot is measured, and the state of the measurement qubit can be inferred[24].

The Pauli exclusion principle states that no two fermions may occupy the same quantum state, i.e., have identical quantum numbers[49]. As the quantum dots are in the single charge carrier regime, there are only two states available: The spin-up and the spin-down state, which can be seperated in energy by Zeeman splitting (See Section 2.3.3), due to the application of a magnetic field.

We can now introduce the concepts of the auxillary qubit and the measurement qubit. The auxillary qubit is a qubit which is initialised into a known state; the spin-down state, which can be realised simply by waiting, as the auxillary will relax into the energitically favourable state, which fulfills DiVincenzo criteria no. 2. The measurement qubit is the qubit we wish to measure, which has completed some quantum operation, and is ready for read-out. The measurement qubit is then coupled to the auxillary qubit, such that it is energitically favourable for both qubits to exist in the auxilliary dot, signified by the blue star in Figure 3, **c**. The measurement qubit will only be able to exist in the auxilliary dot, if it is in the spin-up state. This is exemplified in Figure 3, **b**. The resulting configuration of qubits, either (2,0) (Unblocked) or (1,1) (Blocked), will alter the measured current through the sensor dot, which can be read out, and the spin state of the measurement qubit can thus be inferred.

2.2.3 Radio-Frequency Reflectrometry

To perform fast and sensitive qubit read-out, a radio-frequency reflectrometry scheme can be employed[50,51]. This is a technique where a radio-frequency signal is sent to the the sensordot, and the reflected signal is measured. The reflected signal will depend on the conductance of the sensordot, and can be used to determine the charge state of the quantum dot.

Generally, this is done to overcome the limitations of DC sensing, which is slow and noisy, as the noise scales with $\frac{1}{f}$. The radio-frequency reflectrometry scheme is much faster and more sensitive, and can be used to perform fast and accurate gate operations and read-out of the qubit state.

The scheme is implemented by connecting an LC (tank) circuit, which is a resonant circuit, to the quantum dot. The tank circuit has a characteristic resonance frequency, which is determined by the inductance and capacitance of the circuit.

$$f_R = \frac{1}{2\pi\sqrt{LC}} \tag{2.1}$$

Where L is the inductance of the circuit, and C is the capacitance of the circuit. As charge occupations change in the quantum dots, so too will the total capacitance of the system, due to a change in quantum capacitance, C_q, which is the capacitance from single charge-carriers. This change leads to a change in the load impedance, Z_L, which therefore has two impacts on the system: The change in the resonance frequency of the tank circuit, and the change in the reflected signal.

$$f_R = \frac{1}{2\pi\sqrt{L(C + C_q)}} \tag{2.2}$$

$$\Gamma_R = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2.3}$$

Γ_R is the reflection coefficient with $\Gamma_R \in [0, 1]$, where 1 is a perfect reflection, and 0 is a perfect transmission. Z_0 is the characteristic impedance of the electronics, which is usually an industry standard of 50 Ω.

Thusly, by sending a probe-tone through the circuit, and measuring the reflected signal, one can determine changes in the occupational states of the quantum dots[11,52,53] .

2.3 Bulk Germanium, Strained Germanium, and the Germanium Heterostructure.

Up until this point, the discussion has been reasonably platform-agnostic.

Let us now introduce the platform of choice for this thesis as a whole, and go through why the germanium heterostructure is used in the first place.

The heterostructure[50,35,24,54,55] that is used for in this work can be seen on Figure 4. The pure, strained germanium has a type I band alignment, which can be seen on Figure 5, **b** and **c**, with its surrounding alloys, meaning holes can be well defined and constrained in the germanium layer, by using a confining potential.

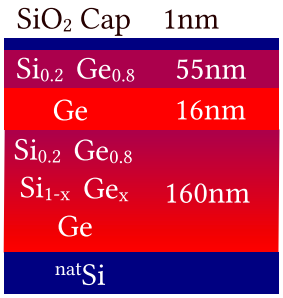

Figure 4

The heterostructure containing the germanium quantum well. Adapted from[24]

There is a silicon-dioxide passivation layer on top of the heterostructure, which is common for these types of structures, as germanium and its alloys have poor native oxides, which can lead to defect surface states that can degrade the performance of the device. The passivation layer is also used to protect the surface of the heterostructure from contamination, and to provide a clean surface for the deposition of the gate electrodes.

Before we delve into the specifics of the heterostructure, we must first understand the properties of bulk germanium, and how the heterostructure and its band alignment is used to confine holes in the germanium layer.

By investigating the charge carrier properties of bulk germanium, we can understand the effects of spin-orbit coupling on the valence band charge carrier states, and how the degeneracies in the valence band can be lifted by the introduction of the heterostructure and a confining potential from a top-gate.

2.3.1 Bulk Germanium

Most metals brought into ohmic contact with germanium exhibits the property of Fermi-level pinning at the valence band[56,57], meaning that the electrons in germanium can be excited into the conduction band, thereby leaving the pseudo-particle, the hole, as the main charge carrier. We will now investigate the properties of holes in the valence band, and why they are a suitable qubit platform.

The electronic band structure of bulk, unstrained germanium, when accounting for degrees of freedom provided by spin and the p-type orbital, should be six-fold degenerate in the valence band at the Γ-point, in the absence of spin-orbit interaction (SOI).[24,6] .

The spin-orbit interaction lifts some of these degeneracies, which is crucial when trying to find an isolated, minimally coupled quantum mechanical two-level system, which is the basis of a qubit.
We can derive the effects of the spin orbit operator on the valence band, $\delta_{SO}\boldsymbol{L}\cdot\boldsymbol{S}|\Psi\rangle$, by investigating commutative relationships after having added spin-orbit coupling. The coupling results in a Hamiltonian which no longer commutes with the angular momentum operator, $\boldsymbol{L}$, or the spin angular momentum operator, $\boldsymbol{S}$, but instead commutes with the total angular momentum operator, $\boldsymbol{J}=\boldsymbol{L}+\boldsymbol{S}$. By taking $\boldsymbol{J}^2=(\boldsymbol{L}+\boldsymbol{S})^2 \Rightarrow \boldsymbol{L}\cdot\boldsymbol{S}=\frac{1}{2}(\boldsymbol{J}^2-\boldsymbol{L}^2-\boldsymbol{S}^2)$, invoking the standard eigenvalue equations[12,24] for various momentum operators, $\boldsymbol{J}^2|\Psi\rangle=\hbar^2 j(j+1)|\Psi\rangle$, $\boldsymbol{S}^2|\Psi\rangle=\hbar^2 s(s+1)|\Psi\rangle$, and $\boldsymbol{L}^2|\Psi\rangle=\hbar^2 l(l+1)|\Psi\rangle$, it follows that:

$$\delta_{SO}\boldsymbol{L}\cdot\boldsymbol{S}|\Psi\rangle = \frac{\hbar^2\delta_{SO}}{2}(j(j+1)-l(l+1)-s(s+1)|\Psi\rangle \tag{2.4}$$

The quantum number j assumes the range $|l-s| \leq j \leq l+s$, in integer steps. As we are interested in charge carriers of spin-half, $s=\frac{1}{2}$, and p-type orbitals, $l=1$, this results in: $j=\frac{3}{2}$ and $j=\frac{1}{2}$. This results in four valid states for $j=\frac{3}{2}$, since $m_j \in [-j,j]$, and two valid states for $j=\frac{1}{2}$.
The states are:

$$\left|\frac{3}{2},m_{\frac{3}{2}}\right\rangle = \left\{\left|\frac{3}{2},-\frac{3}{2}\right\rangle,\left|\frac{3}{2},-\frac{1}{2}\right\rangle,\left|\frac{3}{2},\frac{1}{2}\right\rangle,\left|\frac{3}{2},\frac{3}{2}\right\rangle\right\} \tag{2.5}$$

$$\left|\frac{1}{2},m_{\frac{1}{2}}\right\rangle = \left\{\left|\frac{1}{2},-\frac{1}{2}\right\rangle,\left|\frac{1}{2},\frac{1}{2}\right\rangle\right\} \tag{2.6}$$

By allowing the spin-orbit operator from Equation (2.4) to act on these states, we find that:

$$\delta_{SO}\boldsymbol{L}\cdot\boldsymbol{S}\left|\frac{3}{2},\pm\frac{3}{2}\right\rangle = \frac{\delta_{SO}}{2} \quad \& \quad \delta_{SO}\boldsymbol{L}\cdot\boldsymbol{S}\left|\frac{3}{2},\pm\frac{1}{2}\right\rangle = \frac{\delta_{SO}}{2} \tag{2.7}$$

$$\delta_{SO}\boldsymbol{L}\cdot\boldsymbol{S}\left|\frac{1}{2},\pm\frac{1}{2}\right\rangle = -\delta_{SO} \tag{2.8}$$

producing a four-fold degeneracy for the $j=\frac{3}{2}$ states, a two-fold degeneracy for the $j=\frac{1}{2}$ states, and a spin-orbit gap of $\Delta_{SO}=\frac{3\delta_{SO}}{2}$.

From this point, the $\left|\frac{3}{2},\pm\frac{3}{2}\right\rangle$ states are referred to as the heavy hole (HH) states, and the $\left|\frac{3}{2},\pm\frac{1}{2}\right\rangle$ are referred to as the light hole (LH) states. This terminology will be explained in the next section.

As there are still too many degeneracies in the system for it to be utilised as a spin-qubit, we introduce the germanium heterostructure, which can be seen on Figure 4. The heterostructure is a strained germanium layer, sandwiched between silicon-germanium alloys, which allows for the confinement of holes in the strained germanium layer.

2.3.2 Confinement

To understand how the addition of confinement in the system lifts degeneracies between the HH and LH states, we investigate a simplified version of the Luttinger-Kohn Hamiltonian[6,58,59,60], which is often used to describe the hole properties at the top of valence bands in quantum-well semiconductors. In this work[54,61], we make use of a spherical approximation, due to the substrates being grown on the high symmetry [001] crystallographic axis[6,62,63], such that the Luttinger-Kohn Hamiltonian is as follows:

$$H_{LK} = -\frac{\hbar^2}{2m_0}\left[\left(\gamma_1+\frac{5}{2}\gamma_S\right)k^2 - 2\gamma_S(\boldsymbol{k}\cdot\boldsymbol{J})^2\right] \tag{2.9}$$

Where γ_1 and γ_S are material Luttinger parameters, m_0 is the free electron mass, $\boldsymbol{k}^2=k_x^2+k_y^2+k_z^2$ where k, is the crystal momentum and $\boldsymbol{J}$ is the total angular momentum.

Allowing this Hamiltonian to act on the HH and LH states, yields two sets of two-fold degenerate eigenenergies:

$$|m_j\rangle = \left|\pm\frac{3}{2}\right\rangle \Rightarrow E_{HH} = \frac{-\hbar^2k^2}{2m_{HH}}, \quad m_{HH} = \frac{m_0}{\gamma_1-2\gamma_s} \tag{2.10}$$

$$|m_j\rangle = \left|\pm\frac{1}{2}\right\rangle \Rightarrow E_{LH} = \frac{-\hbar^2 k^2}{2m_{LH}}, \quad m_{LH} = \frac{m_0}{\gamma_1 + 2\gamma_s} \tag{2.11}$$

By substitution of the material Luttinger parameters found in Germaniun[6,64], $\gamma_1 \approx 13$ and $\gamma_s \approx 5$, we find that: $m_{HH} = 0.33m_0$ and $m_{LH} = 0.04m_0$

From these eigenenergies and effective masses, it is quick to see why the nomenclature designates them as heavy and light holes, and that while degenerate at the Γ-point, the degeneracies are lifted when $\boldsymbol{k} \neq 0$.

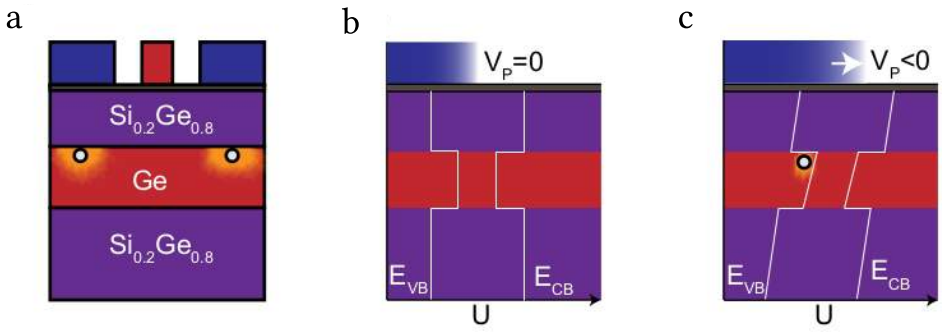

Figure 5 **a**: Germanium/silicon-germanium heterostructure, in a cross-sectional view with a layer of gates on top, showcasing the position of the charged particle, in this instance a hole, based on the potential of the gates. **b**: A band diagram of the heterostructure, showcasing the band structure of the materials at zero potential from gates. **c**: A band diagram of the heterostructure, showcasing the band structure of the materials at a potential from the gates. Adapted from[24]

However, the effects of the heterostructure has still not been taken into account. Due to the type I[61] zero-field band alignment of the heterostructure, (See Figure 5, **b**), and the applied confining potential's effect on said band structure (Figure 5, **c**), there is a strong confinement of holes to the top of the Ge layer, which leads to a quantisation of the z-component of the crystal momentum, such that: $k_z = \frac{\pi n}{d}$, where $n \in \mathbb{N}$ is an excitation harmonic number, and d is the diameter of the quantum dot. This quantisation leads to the degeneracy being lifted, which is evident when looking at the eigenenergies, which are quantised in the z-direction, but continuous in the x and y directions.

$$E_{HH} = -\frac{\hbar^2}{2m_0}\left(k_\parallel^2(\gamma_1 - 2\gamma_s) + \frac{n_{HH}^2\pi^2}{d^2}(\gamma_1 - 2\gamma_s)\right) \tag{2.12}$$

$$E_{LH} = -\frac{\hbar^2}{2m_0}\left(k_\parallel^2(\gamma_1 + 2\gamma_s) + \frac{n_{LH}^2\pi^2}{d^2}(\gamma_1 + 2\gamma_s)\right) \tag{2.13}$$

where $k_\parallel^2 = k_x^2 + k_y^2$, and n_{HH} and n_{LH} are the excitation harmonic numbers for the HH and LH states, respectively.

Even at $\boldsymbol{k}_\parallel = 0$, the degeneracies are lifted, due to the confinement in the z-direction. Defining the energy gap as:

$$\Delta_{LH,HH} = E_{HH} - E_{LH} = \frac{2\gamma_s\hbar^2\pi^2}{m_0 d^2} \tag{2.14}$$

Another interesting feature of this, is that the HH and LH states switch effective masses, such that the HH state now has the lightest effective mass, and the LH state is the heaviest.

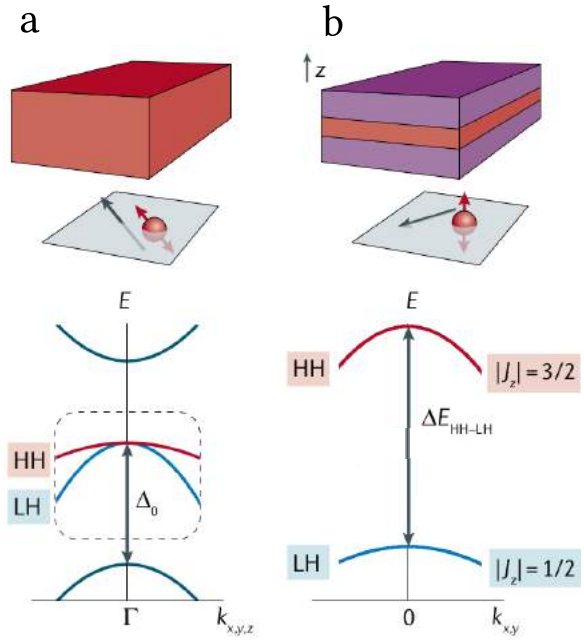

Figure 6: Bulk and Confined germanium Valence Band Structure.

a: Showcases the bulk structure, along with the quantisation axis and direction of motion, and the degeneracy of the HH and LH states. **b**: Showcases the heterostructure, with the confinement leading to a locked quantisation axis and an in-plane direction of motion, while lifting of the degeneracy of the HH and LH states. The energy seperation between the HH and LH states is defined as $\Delta E_{\text{HH-LH}}$. Adapted from[6]

While a full description of the underlying physics is outside the scope of this thesis, there is another factor in this platform that further splits the HH and LH states, which is the strain induced by a lattice mismatch between the $Si_{1-x}Ge_x$ alloys and the pure Ge layer. This is modelled by adding a Bir-Pikus strain Hamiltonian[58], which induces an additional HH-LH energy splitting of Δ_{strain}, which for the heterostructure specific to this thesis, is on the order of $\Delta_{\text{strain}} \approx 50$ eV[24].

2.3.3 Spin-Orbit Coupling and Zeeman Splitting

While the platform has managed to lift almost all degeneracies in the system, there is still one left: spin degeneracy. This is lifted by the introduction of an external magnetic field. We then take a closer inspection of the effects of the spin-orbit interaction on the HH states.

Due to the confining potential, the material has a structural inversion asymmetry (SIA), which induces a spin-orbit interaction known as the Rashba spin-orbit interaction, whose Hamiltonian is given by[24,65,66]:

$$H_{SO,R} = i\alpha_{R2}(k_+^3\sigma_- - k_-^3\sigma_+) + i\alpha_{R3}(k_+\sigma_+ - k_-\sigma_-)k^2 \tag{2.15}$$

where α_{Rj} is the j'th Rashba strength coefficient, deciding the weight of the interaction, and $\sigma_\pm = \sigma_x \pm i\sigma_y$. While the system also does contain a term linear in k, whose strength is governed by the Rashba coefficient, α_{R1}, it is usually much smaller than the cubic terms, and is thusly neglected[65]

In these systems, and under the spherical assumption of the Luttinger-Kohn Hamiltonian, the α_{R2} term usually dominates the interaction[65]. The introduction of an external magnetic field, causes the Zeeman Hamiltonian for holes in the upper valence band to be given by:

$$H_Z = -2\kappa\mu_B \boldsymbol{B}\cdot\boldsymbol{J} - 2q\mu_B \boldsymbol{B}\cdot\boldsymbol{J}^3 \tag{2.16}$$

where μ_B is the Bohr magneton, $\boldsymbol{B}$ is the magnetic field, and κ and q are Luttinger parameters. Looking explicitly at heavy holes, we find:

$$H_Z = -\left(3\kappa + \frac{27}{4}q\right)\mu_B B_z \sigma_z - \frac{3}{2}q\mu_B(B_x\sigma_x - B_y\sigma_y) \tag{2.17}$$

from which the g-factors are read off as:

$$g_z = g_\perp = 6\kappa + \frac{27}{2}q \quad \text{and} \quad g_x = g_y = g_\parallel = 3q \tag{2.18}$$

From this it is quite evident, that the g-factor in the material is heavily anisotropic, and the effect of an externally applied magnetic field will depend heavily on its orientation.
While a perpendicular magnetic field is indeed utilised in this work, it is with regards to a Quantum Hall Effect (See Section 2.4), in which the lifting of the spin degeneracy is not of great importance. Therefore, we are restraining ourselves to the treatment of the in-plane magnetic field. For this specific case, the Zeeman splitting of the heavy holes is perturbed by a spin-orbit term, which is given by[67]:

$$H_{SO,Z} = \frac{3\gamma_s \kappa \mu_B}{m_0 \Delta_{HH,LH}}(B_- k_-^2 \sigma_+ + B_+ k_+^2 \sigma_-) \tag{2.19}$$

where $B_\pm = B_x \pm iB_y$ and $\sigma_\pm = \sigma_x \pm i\sigma_y$.

For the complete spin-splitting Hamiltonian, we find:

$$\begin{aligned} H_{SO} = {} & i\alpha_{R2}(k_+^3\sigma_- - k_-^3\sigma_+) + i\alpha_{R3}(k_+\sigma_+ - k_-\sigma_-)k^2 \\ & + \frac{3\gamma_s\kappa\mu_B}{m_0\Delta_{HH,LH}}(B_- k_-^2\sigma_+ + B_+ k_+^2\sigma_-) \end{aligned} \tag{2.20}$$

This is a crucial result, as it shows that the Zeeman-splitting of the heavy holes is dependent on the confining potential, and even more so, the g-factor becomes electrically tunable. However, this also carries a disadvantage, as the eigenenergies of the HH states are now dependent on electric fields, introducing a source of decoherence: Charge noise. This turns out to be one of the major sources of decoherence in the Ge/SiGe qubit platform[54].

2.3.4 Electric Dipole Spin Resonance

As seen in the Section 2.3.1 - 2.3.c, the spin-orbit interaction plays a perturbative role role in defining the proper system for a spin qubit. A closer inspection reveals that SOI also allows for the manipulation of the spin qubit, through the use of electric fields oscillations. This is known as electric dipole spin resonance (EDSR)[67,24]. The EDSR is a technique that allows for the manipulation of the spin qubit by applying an oscillating electric field, which couples to the spin of the hole, and drives transitions between the spin states. While a proper, technical derivation of the EDSR is outside the scope of this thesis, we will provide a brief overview of the technique, and how it is used in the Ge/SiGe qubit platform.

Investigating the spin transitions a bit more closely, via the eigenstates of the system which are given by a product of Fock-Darwin and spin states: $|n, l, j\rangle$, where $n \in \mathbb{N}$ is the principal quantum number, and $|l| \leq n$ is the azimuthal quantum number. The eigenstates of the system with a vanishing spin-orbit interaction, $H_{SO} = 0$, are given by: $|0, 0, \pm\frac{3}{2}\rangle$, between which spin transitions cannot be driven by a magnetic dipole interaction, due to $\Delta m_j = 3$[12]. The two-fold degeneracy of the Fock-Darwin spectrum is lifted by a Zeeman splitting for a finite magnetic field, as seen in Section 2.3.3. By then incorperating the SOI as a perturbation, we see that the α_{R2} cubic Rashba term from Equation (2.20) actually couples the ground state, $|0, 0, \pm\frac{3}{2}\rangle$, with the first orbital excitation, $(n = 1)$ with opposite spin-sign, which allows for the driving of spin transitions by an oscillating electric field.

The oscillating electric fields needed for EDSR can be readily produced by the gate electrodes, already used to define the quantum dots.

2.3.5 A Quantum Dot in the Germanium Heterostructure

Following the introduction of the germanium heterostructure, and the effects of the confinement and the spin-orbit interaction, we can now introduce the formalism for a single quantum dot coupled to a resevoir and a drain.

Generally, in order to observe the single-charge carrier regime in transport, we need to consider the energy scales involved. As a rule of thumb, this does not occur unless the Coulomb energy is the dominating energy scale[68,69].

The source and the drain both have a chemical potential, μ_S and μ_D, respectively, which can be controlled with a bias voltage across the two, as described in Section 2.2.1. We now investigate the Coulomb energy of a single quantum dot.

The quantum dot is a disc, with radius r, embedded in a homogenous dielectric material with relative dielectric constant ε. We can then write the self-capicitance of such as a disc as:

$$C = 8\varepsilon\varepsilon_0 r \tag{2.21}$$

Assuming the island hold N number of charges, The Coulomb energy is then given by:

$$E_{\text{elstat}}(N) = \frac{e^2N^2}{2C} = \frac{e^2N^2}{16\varepsilon\varepsilon_0 r} \tag{2.22}$$

As we are interested in continuously loading or unloading charges, we can write the charging energy as:

$$E_C(N+1) = E_{\text{elstat}}(N+1) - E_{\text{elstat}}(N) = \frac{e^2}{C}\left(N + \frac{1}{2}\right) \approx \frac{e^2}{C}N = \frac{e^2}{8\varepsilon\varepsilon_0 r}N \tag{2.23}$$

where we have assumed that $N \gg 1$. Traditionally, however, the charging energy is defined as the difference:

$$\Delta E_C = E_C(N+1) - E_C(N) = \frac{e^2}{C} = \frac{e^2}{8\varepsilon\varepsilon_0 r} \tag{2.24}$$

We must also take into account the other energy scales involved, one of which, is the confinement energy of quantum states in the quantum dot. We can estimate this confinement energy as:

$$E_{\text{conf}}(N) = \frac{\hbar^2}{2m^*r^2}N^2 \tag{2.25}$$

Where m^* is the effective mass. From which we see that the confinement energy scales with the square of the number of charges in the quantum dot. However, the above expression only holds true for materials with a parabolic dispersion relation, which is exactly the case of silicon and germanium. We can estimate the single-particle level spacing by utilising a quantum mechanical harmonic oscillator. The spatial extent of the ground state of said oscillator, is given by:

$$2r = \sqrt{\frac{\hbar}{m^* \omega_0}} \tag{2.26}$$

Where ω_0 is the frequency of the oscillator. From this, we can derive the characteristic energy scale as:

$$\Delta = \hbar\omega_0 = \frac{\hbar^2}{4m^* r^2} \tag{2.27}$$

which we can see scales inversely with the square of the radius.

A typical value of the radius of a quantum dot in this work is 180 nm, and the effective mass[70] of the HH state is approximately $m^* = 0.08m_0$, in a strained, planar germanium quantum well. For these values we are given a ground state energy of:

$$\Delta \approx 20 \ \mu\text{eV} \tag{2.28}$$

Going back to Equation (2.24), inserting the value of relative permittivity for Al_2O_3, $\varepsilon_{\text{Alumina}} = 10.07$ (see Section 3.2.2), with a radius of 180nm, grants us a charging energy of approximately $\Delta E_C \approx 1.25$ meV. From this, it is evident that the charging energy dominates the energy scale.

Each energy E_N will depend on the voltage applied to the plunger gate. By setting a particular $V_{pg} = V_{pg}^0$, and expanding in a small range around around it, we find:

$$E_N(V_{pg}) = E_N(V_{pg}^0) - |e|N\alpha\Delta V_{pg} \tag{2.29}$$

where $\Delta V_{pg} = V_{pg} - V_{pg}^0$, and α is the lever-arm.

We can then define the chemical potential of the quantum dot to be:

$$\mu_N(V_{pg}) = E_N(V_{pg}) - E_{N-1}(V_{pg}) \tag{2.30}$$

By then combining Equation (2.29) and Equation (2.30), we find that the chemical potential of the quantum dot, as controlled by the plunger gate voltage, is:

$$\mu_N(V_{pg}) = \mu_N(V_{pg}^0) - |e|\alpha\Delta V_{pg} \tag{2.31}$$

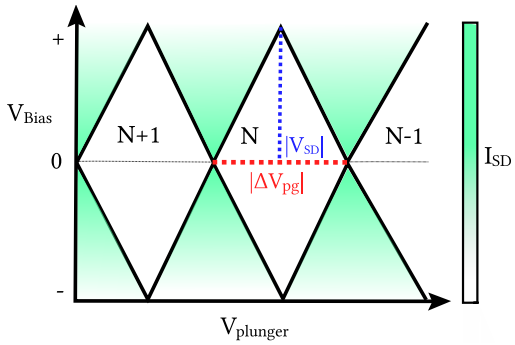

Figure 7:

2D scan of the current I_{SD} as a function of bias voltage, V_{SD}, and plunger gate voltage, V_{pg} showcasing Coulomb diamonds. Adapted from[50].

Based on this, we can extract both the charging energy and the lever-arm from a measurement of Coulomb diamonds, which are the regions in the charge stability diagram where the current is suppressed due to the Coulomb blockade effect. By relation is the following:

$$|\Delta V_{pg}| = \frac{|V_{SD}|}{\alpha} \tag{2.32}$$

where $|V_{SD}|$ is the absolute value of the source-drain voltage, where the Coulomb oscillations have the sharpest peaks, and $|\Delta V_{pg}|$ is the difference in top-gate voltage between two peaks.

2.4 The Quantum Hall effect

The full description of the Quantum Hall effect is outside the scope of this thesis, but a brief overview will be given here, as it has been used to characterise the heterostructure used in this work.

The Quantum Hall effect[71] is a quantum mechanical phenomenon that occurs in 2D charge carrier systems in the presence of a magnetic field, and at sufficiently low temperatures, where the thermal energy scale set by $k_B T$ is significantly smaller than the Landau level spacing, $\hbar\omega_C$, where ω_C is the cyclotron frequency. It consists of a quantisation of the Hall resistivity, ρ_{xy}, in reciprocal units of the conductance quantum, $\frac{e^2}{h}$, which is in stark contrast to the classical picture, where it is linear in applied perpendicular magnetic field, $B_\perp$.

It is characterised by the plateaus in the Hall resistivity, ρ_{xy}, at particular values of the filling factor in the form of $\frac{1}{\nu}$, and the oscillations in the longitudinal resistivity, ρ_{xx}, in areas of a steep incline in the Hall resistivity.

The filling factor ν is a measure of the filling of the various Landau levels (LLs).

One can measure the Hall resistivity, $\rho_{xy} = \frac{V_{xy}}{I_{\text{sd}}}$, and the longitudinal resistivity, $\rho_{xx} = \frac{V_{xx}}{I_{\text{sd}}} \times \frac{L}{W}$, where V_{xx} and V_{xy} are the voltages across the Hall probes, I_{sd} is the source-drain current, and $\frac{L}{W}$ is the geometric factor of the probe (See Figure 33). From these, one can extract the active carrier density, p_{2D}, the mobility, μ, the conductance, σ_{xx}, and ultimately the percolation density, p_p, thereby characterising the material properties of the heterostructure.

The active carrier density, p_{2D}, can be calculated in the linear regime of the Hall resistivity, via the relation

$$\rho_{xy} = \frac{B}{e p_{2D}} \tag{2.33}$$

in the low magnetic field limit ($B > 0.3\ T$). ρ_0 was extracted from ρ_{xx} at 0 magnetic field.
The mobility, μ, can be calculated from the relation

$$\frac{1}{\rho_{xx} e} = p_{2D}\mu \tag{2.34}$$

The conductivity, σ_{xx}, can be calculated from the inverse relation with the longitudinal resistivity, ρ_{xx}. And finally, the percolation density, p_p, can be inferred from a power law fit, according to percolation theory[61], where the conductivity is fit to a power law of the form:

$$\sigma_{xx,fit} = A\left(p_{2D} - p_p\right)^k \tag{2.35}$$

where the percolation density, p_p, is the point at which the conductivity is zero, giving an indication of the lowest charge-carrier density at which the system is conducting.

A note can also be made on the limiting factor of the mobility in the system. By fitting the non-saturated regime of the mobility as a function of p_{2D}, according to a power law:

$$\mu_{fit} = B \cdot p_{2D}^a \tag{2.36}$$

one can extract the limiting factor of the mobility, according the numerical value of the power, a. More on this in section Section 5.1.1.

2.5 The 2×N Quantum Dot Array and Its Parametric Design

The design of a scalable quantum computer is a challenging task, as it requires the ability to control and manipulate a large number of qubits, while maintaining the ability to perform fast and accurate gate operations, and read-out of the qubit state. Although individual control of each barrier gate, is not strictly necessary[72], it is a desirable feature, as it allows for complete control of the device.

Below, we will discuss the design of a 2×N quantum dot array, which is a scalable design that allows for the individual control of each gate electrode, and can be extended to a larger array of quantum dots (See Section 2.5.4), while maintaining the ability to perform fast and accurate gate operations and read-out of the qubit state.

By confining the dimensionality to the quasi 1-dimensional array of a 2×N structure, we can adhere to the strict fabricational constraints of such nano-scale structures, while maintaining complete, individual control of each gate electrode, in a theoretically scalable design. Recent research has also delved into developing efficient fault-tolerant error correction schemes for such a quasi-1D structure[9], which is essential for the development of a large-scale quantum computer.

Constraining the array to be quasi 1D, allows for a linear increase in gate-number with the number of columns, while maintaining a constant number of rows, given by: $\delta g = 4\delta N + 1$, where δg is the variation in gate-number, and $\delta N \in \mathbb{N}$ is the change in number of columns.

However, even with a simple linear increase in gate-number, the traditional computer-assisted design (CAD) methods, which rely on manual design, quickly become tedious, unmanagable, and error-prone.

This is where the idea of parametric design comes in. Parametric design is a design approach that builds a code-base, utilising a geometry library, such as Phidl[73], to create, relate, and place various geometries with respect to one another. This allows for the creation of designs in a parameter-space, which can easily be modified.

2.5.1 Phidl

Phidl is a geometric design library implemented in Python, which allows the user to create and manipulate 2D geometry by utilising the GDSII stream format. It is a powerful tool for creating complex geometries, and is particularly useful for creating parametric designs, which can be used to create a library of designs that can be easily modified and reused.

This method has a high initial time-cost, compared to the traditional CAD tools such as AutoCAD. However, one gains absolute control and machine-precision over distances, shapes, and positions, that are difficult to obtain using hand-drawn design platforms.

In this work, the initial designs were all “hard-coded”, in the sense that the designs were created by manually placing each gate electrode, and routing the connections between them. This was done to ensure that the designs were correct, and that the parametric design would be able to replicate the designs accurately.

Once the design was finished, it was generalised it in such a way, that changing design features’ shape, relative position, or even number of quantum dots becomes a trivial change of a variable. In this case, the generalisation was done such that the programme reads a YAML file, containing all variables, which is the only file that needs changing, if designs features are needed to be changed. The method provides ease of use, in that no additional coding needs to be done, and the source-code remains closed

for minor changes. The planned extensibility of the designs benefit greatly from the parametric design structure.

The functionality of Phidl is rooted in the geometric library, which is a way of creating object geometries with desirable properties, such as routing ports, layer-specificity, absolute position, and relative positioning. When a geometric object is created, it either has intrinsic ports or seperately created ports are needed. A port is an object used to route geometries between various objects. A rectangle will have 4 ports, one for each side, which can then be routed to any other port in the system. The routing creates another geometric object, also with layer-specificity. Phidl allows for various routing techniques, such as Manhattan routing, straight routing, and custom routing.

An example of the parametric design can be seen on Figure 8, **a**, where everything on the chip, except for the fourth quadrant, was created using the parametric design. The fourth quadrant was created manually, to serve as test-devices, to verify that the parametric design and the fabrication procedure was working as intended.

2.5.2 The AXL MkX Chip Design

There are many considerations to make, when designing a prototype of a scalable, pseudo-1D quantum dot array. The design must be scalable, such that it can be extended to a larger array of quantum dots, while maintaining the ability to individually control each gate electrode. It must also be manufacturable, such that it can be fabricated using standard semiconductor processing techniques.

Figure 8, **a**, shows the full chip design, the various components of which will be explained later on. **b** and **c**, showcases the 2x2 and 2x3 array designs, which are the extent of N attempted in this work. As the chip name suggests, this is the final iteration of 10 differerent designs in total, which have been tested and iterated upon, to ensure that the design is manufacturable, and that the quantum dots can be controlled individually, with minimum leakage between gates.

The design consists of four quadrants, three of which of which contains a 2xN array of quantum dots. The quantum dots are defined by the ohmics, plunger, barrier, and screening gates, which are used to populate the two-dimensional hole gas (2-DHG), control the occupancy of the quantum dots, manipulate the tunneling rate between dots, and to screen the quantum well from the gate-electrode to create a circularly defined potential, respectively. A layer-structure such as this, is referred to as having 1+3 layers, with one ohmic and three top gate layers.

The fundamental difference between this work and previous work[24,50], is the seperation of screening gates and barrier gates. For smaller, less complex design, there is no need to seperate the two, as individual gate contrability is achievable without overlapping gates in the same layer. However, as the design becomes more complex and the number of qubits increase, so too does the number of gates, leading to unmanagably small tolerances for fabrication.

Therefore, while it increases the risk of fabricational error, the seperation of the two gates is a necessary step in the development of a scalable quantum dot array.

The fourth quadrant of the chip contains three Hall bars, and four hole transistors, which are meant to act as test-devices, to ensure that the parametric design is working as intended. This specific quadrant was designed manually.
The Hall bars are used to measure the Hall resistivity (see Section 5.1.1), and the hole transistors (see Section 5.2.1) are utilised as a test-structure for the sensor dots, to see if the design is able to initiate charge carrier transport through the 2-DHG.

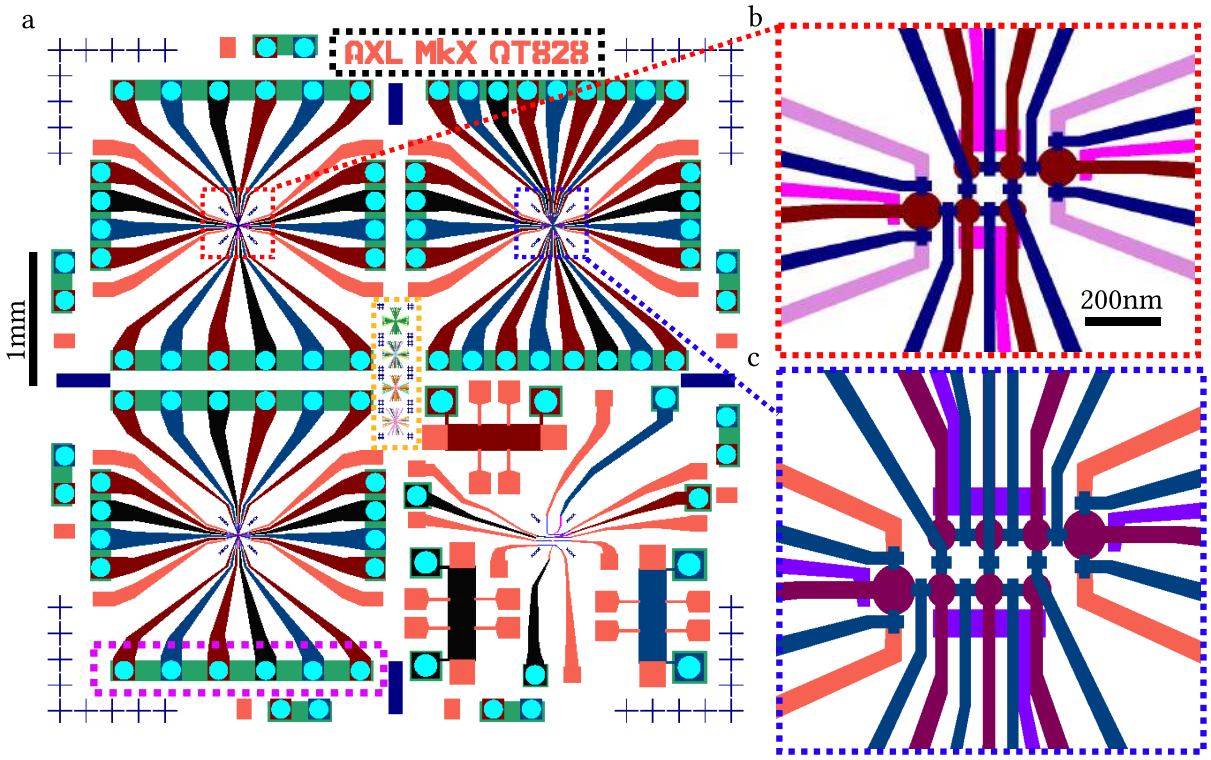

Figure 8 **a**: Full schematic of the AXL MkX chip. Three out of four quadrants have a 2xN array design. The fourth quadrant has 3 Hall bars, and 4 hole transistors, meant to act as test-devices. Black outline: Visual aid. Yellow outline: Test-structures. Purple outline: Buffer stacks, bonding pads, and SiO_2 ridge, as seen from above. **b**: Close-up of the full schematic for the 2x2 design. Fuchsia: Screening gate. Blue: Barrier gate. Red: Plunger gate. Pink: Ohmics. **c**: Close-up of the 2x3 array. Purple: Screening. Blue: Barrier. Burgundy: Plunger. Orange: Ohmics.

For the larger structures on the chip, there are a few components that are crucial for the fabricational process. As seen on Figure 8 **a**, in a black outline, is the name of the chip, which is not just for logging purposes, but a visual aid, such that the orientation of the chip is clear to the naked eye. This is essential when aligning the chip in the various machines used in the fabrication process. The yellow outline contains the test-structures, which are used as a proxy when evaluating the success of a fabricational run. The scanning electron microscope (SEM) and its electron beam, can degrade structures by carbon deposition and charging of the electrically isolated gates, so only the test structures are imaged. The purple outline contains the buffer stacks (teal), bonding pads (red, blue, black), and the SiO_2 ridge (green), as seen from above. The reason for the buffer stack and the SiO_2 ridge will be expanded upon in Section 4.5.1.
Similar, detached, structures can be seen on the edges. These are test bonding-pads, used to calibrate the wire-bonding machine, and to ensure that the wire-bonding is done correctly.

Cross-markers can also be seen in each corner. These are global markers, which are used to align the chip during the fabrication process (See Section 4.1.3). A similar, smaller set of markers can also be seen in the middle of the red outline, which serve a similar, but more precise purpose.

2.5.3 The Parameter Space and Simulation Pipeline

Now that the overall design has been introduced, an introduction to the used parameter space for the parametric design can be given. The parameter space is a set of variables, which are used to define the

geometries of the quantum dot array, and are fully controllable by the user, with the simply changing of a YAML file.

While the parameter space is too large to cover fully, without tedium, a few key parameters will be introduced here.

	Definition	Value used
Angle Resolution	A parameter, which specifies the angularity of rounded figures, i.e., the resolution.	10
Amount of dots	The amount of ordinary quantum dots created by the algorithm	2-3
Dot Radius	The radius of an ordinary quantum dot	120nm
Sensordot Radius	The radius of the sensordot	180nm
Pitch	The distance between each pair of quantum dots. Both in the x- and y-direction.	200nm
Starting Coordinates	Where the first quantum dot will be placed, around which everything else is placed relatively.	[0,0]
Gate width	The width of the electrode, coming out of the central feature. Applies to ohmic, screening, plunger, and barrier gates	42-60nm
Marker width	The width of a marker arm. Parameters exists three types of markes: Global, local, and the inner marker inside a global marker.	1μm
Local Marker Positions	A list of length 4, containing 4 numbers, which indicate the diagonal distance away from the center of the design.	[160, 185, 210, 235] (μm)
Extendibility	A Boolean, which decides whether the design is locked in the x-direction, or if it can expand with the number of qantum dots.	False
Layer List	A list containing a string, and two floats. The string indicates layer name; the two floats indicate layer number and datatype.	[“Name”, Layer Number, 0]

Table 1: Minimised Parameter Space

Minimised parameter space. Key parameters used in the parametric design, and the used value.

These are just 11 out of 126 parameters, which are used to define the geometries of the quantum dot array. The full parameter space can be seen on the GitHub repository[74], where the code and all adjacent material to this work is stored.

Once all parameters have been defined, and a design has been created, the design can immediately be pipelined into a simulation, which is used to evaluate the design, and to ensure that the design is capable of producing the desired results. We delve into this, in the following section.

2.5.4 Further Work

This work has focussed on developing a prototype of a scalable, pseudo-1D quantum dot array. However, the design is not yet fully scalable, as the sensoring capabilities are limited to a 2x3 design. A possible solution to this problem is to implement a more complex sensing scheme, such as a radio-frequency reflectrometry scheme in the form of dispersive sensing[75], which would allow for the sensing of a larger array of quantum dots.

This would require a redesign of the chip, to include the necessary components for the dispersive sensing scheme, such as an extra sources and drains, and several radio-frequency reflectrometry circuits.

3.

Simulations of Electrostatic Potentials in the Quantum Well

Being able to simulate the chip design is an advantage to the design process, as it is possible to test the design before it is actually fabricated. This is especially important when the design is complex and the chip is expensive to produce or limited materials are available as is the case with the specially produced heterostucture used in this work. The *in silico* experiments are performed using the Finite Element Method (FEM)[76,77] . The FEM is a numerical method for dissecting continuous media into a finite amount of elements, which are then considered a system of linear equations, for which various solving methods can then be utilised. This simulation uses the conjugate gradient[78] method to solve the system of linear equations. In this particular simulation, the Poisson equation is solved, based on an applied gate voltage (boundary condition), throughout the heterostructure, to gain insight into how effective the various gate layouts are.

While a complete simulation of the device, including all interactions, gate operations, and the spin qubits themselves, would be ideal, it is outside the scope of this thesis. The simulation is limited to the Poisson equation, which is a good starting point, as it allows for the simulation of the electrostatic potential, such that the initial conditions for the potential wells can be optimised.

3.1 The Poisson Equation in 3D

To understand how an electrostatic field propagates through a medium, the Poisson equation is used. The Poisson equation is a partial differential equation, which can be solved by an FEM scheme. The Poisson equation for an undoped semi-conductor is given by[5]:

$$-\nabla \cdot (\varepsilon_s \nabla \varphi(x)) = q(p(x) - n(x)) \quad \forall x \in \Omega \tag{3.1}$$

where q is the elementary charge, n and p are the electron and hole concentrations, respectively, ε_s is the static permittivity of the medium, φ is the electrostatic potential, and the domain $\Omega \subset \mathbb{R}^3$. **Note**: This form allows ε_s to have a spatial dependence. To solve a differential equation using an FEM scheme, the differential equation must first be cast into its weak form.
Assuming that the static permittivity is spatially independent, the Poisson equation can be written as:

$$-\varepsilon_s \Delta \varphi(x) = q(p(x) - n(x)) \tag{3.2}$$

Wanting to solve this equation on the domain Ω, where $\varphi = 0$ on its boundaries, we derive the weak form thus: Take a trial-function η, such that $\eta = 0$ on $\partial\Omega$, multiply it on both sides, and integrate over the domain:

$$-\varepsilon_s \Delta \varphi(x)\eta(x) = q(p-n)(x)\eta(x) \quad \forall x \in \Omega \tag{3.3}$$

$$-\varepsilon_s \int_\Omega \Delta \varphi(x)\eta(x)dx = \int_\Omega q(p-n)(x)\eta(x)dx \tag{3.4}$$

Employing the identity $\nabla \cdot (\eta \nabla \varphi) = (\nabla \varphi)(\nabla \eta) + \eta \Delta \varphi$ and Green's first identity[79], we rewrite the left-hand side as:

$$\varepsilon_s \int_\Omega \nabla \varphi \nabla \eta dx - \int_{\partial \Omega} (\eta \nabla \varphi) \cdot \boldsymbol{n} dS = \int_\Omega q(p-n)\eta dx \tag{3.5}$$

Since $\eta = 0$ on $\partial\Omega$, the second term on the left-hand side vanishes, and we are left with:

$$\varepsilon_s \int_\Omega \nabla \varphi \nabla \eta dx - \int_\Omega q(p-n)\eta dx = 0 \tag{3.6}$$

Before solving the Poisson equation for the system, a consideration to make is how the gate voltages, i.e., boundary conditions are applied. For a system such as this, it is not simply the gate voltage applied, but a slightly modified field outside the surface. For the Dirichlet boundary condition (DBC) at the electric gates, we define the potential as[5]:

$$\varphi_{DBC} = V_g - \frac{\Phi_m - q\varphi_{ref}}{q} \tag{3.7}$$

where V_g is the applied gate voltage, φ_{ref} is the reference potential, and Φ_m is the metal work function[80]. The refence potential is chosen to be $q\varphi_{ref} = E_0 - E_i(Si)$, where E_0 is the vacuum level, and $E_i(Si)$ is the intrinsic Fermi level of silicon. This choice is made, as it has shown numerical robustness in simulations[5].

3.2 Open-source Implementation

While conventional and commercial tools such as Ansys[81] and COMSOL[82] are available and capable of doing the simulatory work described in this thesis, they are difficult to pipeline and automate, and are not open-source. This makes them difficult to integrate into larger workflows such as for example an automated design scheme, compared to their open-source counterparts. For this reason, and to gain full control over the source-code, it was decided to implement the simulation platform in an open-source workspace.

3.2.1 Initial Considerations and Workspace

A combination of Julia, C++, and Python is used to initiate the files, perform the simulation, and the data-analysis, respectively. The location of the interesting structures to simulate is found within the 2D design file, which is then meshed into 3D, and simulated via FreeFEM++[83], a C++ based open-source FEM-solver. Julia was chosen for its speed compared to Python[84,85] , combined with the high-level syntax allowing for ease of building a simulation pipeline. Python was chosen for its extensive library support, which includes support for various filetypes, which Julia does not yet have due to its immaturity. C++ was chosen for its speed and the availability of FreeFEM++. All following mentioned scripts and software was written by the author, unless otherwise explicitly stated.

Due to the finite machine precision of the software, all designs have been scaled by a factor of a 1000, to accommodate a base unit of μm m instead of nm. All relevant physical properties have recieved an identical scaling.

Note: Only 11 out of 24 gates were tuned to produce the results below, due to high time-cost of manually tuning each gate, indicated by a green, dashed line on Figure 9.

The simulation is initiated by running a Julia script, which reads the 2D design file (.gds) generated by Phidl, as mentioned in Section 2.5.1, and extrudes it into a 3D mesh (.stl, .mesh, .msh, or .step) of the design, based on a user-made configuration file, which includes all the material data, x- and y-coordinates, and other vital information.
The meshing takes all closed loops (gates) defined by the 2D design file and extrudes them into 3D polygons, defining them as closed volumes, where each surface on said volumes are bundled together and defined as a single boundary condition. During the 3D meshing, an interactive graphical user interface (GUI) asks the user to label all gates in the design, such that their boundary conditions can later be called by simply using their assigned label.

The meshing is done using the Julia package `Gmsh.jl`[86]

The mesh is exported to a FreeFEM++ file (.edp), from which the relevant equations are defined, the pertinent surface bundles are loaded, and a problem is defined with the proper boundary conditions. For this scenario, the Poisson equation is solved with the gate voltages ranging from −0.77 V to 1.7 V.

All relevant information is saved in .dat files, which are then read by Python for post-processing and visualisation.

3.2.2 System Parameters and Results

Physical constants of the materials, such as the static permittivity, ε, metal work functions, φ, and the intrinsic Fermi level of Silicon, $E_i(\mathrm{Si})$ are set to their table values[87].

	ε	Φ (eV)
Ge	16 ± 0.3	N/A
Si	12.1	N/A
SiGe	$12.1 + x \cdot 3.9$	N/A
Al_2O_3	$\varepsilon_{11} = \varepsilon_{22} = 9.34, \varepsilon_{33} = 11.54$	N/A
Pd	N/A	5.22
Ti	N/A	4.33

Table 2: Table of Physical Constants

Physical constants of the various materials used in this thesis work. x is the percentage of Germanium in the alloy.

Table 2 shows the various physical constants, needed for the simulation. The expression for the static permittivity of SiGe is taken from linear interpolation of the dielectrive constants of the constituents of the alloy. The electron and hole concentrations are set to 0.0, as the system is undoped.
A few simplifications have been made in the simulation to drastically decrease complexity: The static permittivity is set to be spatially independent, and an average value 10.07 has been chosen for Al_2O_3. As the top gates consist of both Ti and Pd, a weighted work function has been calculated, by the percentage of material used compared to the total amount. $\overline{\Phi} = 5.22 \cdot x_{Pd} + 4.33 \cdot x_{Ti}$, where x_{Pd} and x_{Ti} are the percentages of Pd and Ti, respectively.

Figure 9, **a**, shows the design used in the simulation with the manually tuned gates designated by a green-dashed line, with **b**, the electric potential at the 2DEG surface of the Germanium heterostructure. **b** has the full x-y range simulation, with a cut-off of 0.0 V. The red-dashed line indicates a lower cut-off value, whereas the center green-dashed line is the same plot, but projected onto the y-axis, to give a clearer image of the barrier between the potential wells. The sensor-plunger, regular plunger, and all adjacent barrier and screening gates have been tuned to produce these, as outlined by the dashed-green line in **a**. As can be seen from **b**, the potential wells are well-defined, and would be a suitable platform for a quantum dot.
To demonstrate a workable lever-arm for the interdot barrier gate, the simulation is run iteratively, while the gate voltage is swept towards 0 V. As can be seen on Figure 10, **a**, the two potential wells are being hybridised, as the interdot barrier gate, SP1PB, is being swept towards zero. This is indicative

of a well-performing system, in which the potetential barrier between the dots can be controlled, and tuned to a specific tunnel-coupling.

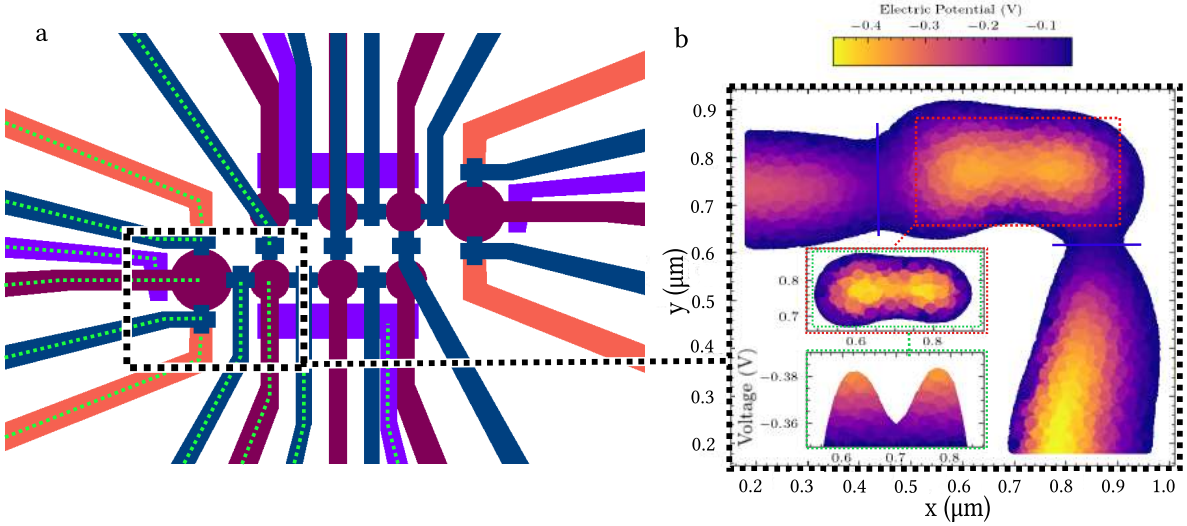

Figure 9 **a**: Cut-out of the simulated design. Tuned gates indicated by dashed, green line. **b**: Colourmap of the electric potential, measured in Volts (V), at the 2DEG of the Germanium heterostructure, where a sensor-plunger, a regular plunger, and all adjacent barrier and screening gates, including the ohmics, have been tuned to produce two potential wells. The black-dashed line indicates the inner parts of the simulated gates, and the red-dashed line indicates a zoom-in on the two potential well, and the green-dashed line is identical, but projected onto the y-axis. The solid green lines indicate the pinch-off region, where the DQD system is pinched off from the their respective gates.

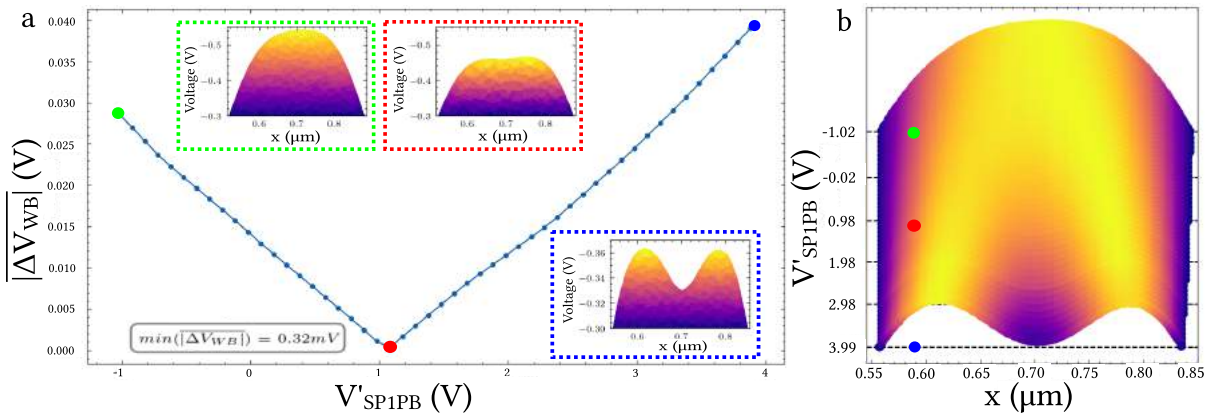

Figure 10 **a**: The absolute, average difference in potential between the two potential wells, as a function of the corrected gate voltage, from Equation (3.7). The blue circle and dashed line, indicate the gate voltage at which the two wells are well-defined and have a barrier between them. The red circle and dashed line, indicate the inflection point and gate voltage at which the two dots are fully hybridised. The green-dashed line and green circle, indicate the gate voltage at which the two dots have merged. **b**: A ridge-line sketch plot, showing the full potential landscape at each dot-pair, for each value of the gate voltage. **Note**: The heights of each trace, i.e., the potential values, are not true to their respective aspect ratios. Each trace has been normalised to 1. It is a sketch to underline the lowering of the barrier, with respect to the potential wells. To note the true value, see inserts on **a**.

This is perhaps more easily visualised on Figure 10, **b**, showcasing a normalised ridge-plot, in which the maximum barrier regime, full hybridised regime, and complete merger regime are outlined.

The wells, shown in yellow, can be seen the move towards full merger as the barrier gate is swept.

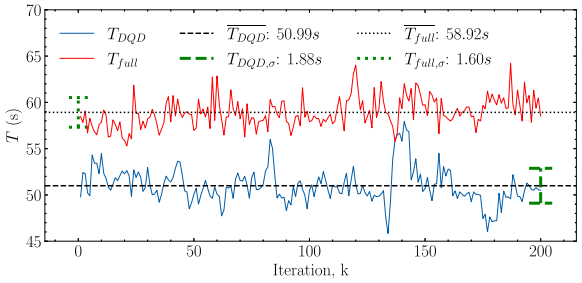

Figure 11: Benchmarking

Simulation time, T_{DQD} and T_{full} as a function of iteration, in which each gate voltage is assigned a random value in the range [−2.0, 2.0] V, for each iteration. T_{DQD} is for 11 gates, whereas T_{full} is for all 24 gates.

To ensure stable convergence of the conjugate gradient method, at all possible gate voltages, benchmarking was performed. This was done by assigning each of the 11 gates voltage to a random value in the range [−2.0, 2.0] V, and bench-marking the simulation time against CPU clock-time; iterating over this process 200 times. The simulation time, T_{DQD}, can be seen on Figure 11, where T_{DQD} is plotted against the iteration integer, k. The simulation time is stable, with a mean of approximately 51 s, and a standard deviation of 1.88s. This shows that the simulation is stable and converges well, for the expected range of boundary conditions. To ensure that the simulation would converge for the full set of gates, the same benchmarking is performed for all 24 gates, and the results are shown in Figure 11. T_{full} shows the same stability, albeit at a slightly higher mean of ~59 s, which is to expected. Meaning, that for the simulation to run with approximately twice the amount of active gates, it only adds ~8 seconds to the total simulation time.

3.3 Further Work

3.3.1 Extension to Self-Consistent Poisson-Schrödinger Equation

The simulation is currently only able to simulate the Poisson equation, but the platform would be well suited to extend this to simulate a self-consistent Poisson-Schrödinger equation, which would allow for the simulation of charge-carrier densities and wavefunctions. This would provide a more accurate representation of the system, as it would allow for the simulation of quantum dots, which are the main foci of this work.

To be able to do this, and to ensure convergence[5,88], a predictor-corrector (P-C) scheme could be implemented. Figure 12 shows a sketch of the workflow of such a scheme.

This scheme was attempted in the thesis work, but it proved to be difficult to implement, as the method used to solve the Poisson equation was not compatible with the Schrödinger equation, as it had difficulty in solving complex problems. The platform, however, is capable of performing such tasks, and it is recommended that this is implemented in future work.

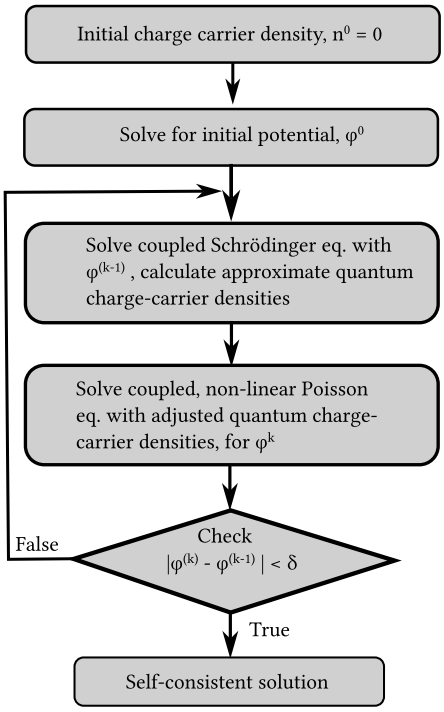

Figure 12: P-C Sketch

Sketch of the workflow in a predictor-corrector scheme, for solving the self-consistent Poisson-Schrödinger equation.

3.3.2 Automated Design Using Machine Learning

The reason for implementing this entire simulation platform in an open-source workspace, was to gain pipeline and automation capabilities, which would allow for the simulation to be implemented in a larger workflow, such as a machine-learning algorithm, which would have two main functions: [1]: To optimise the gate voltages to a produce the desired potential wells, and [2]: To optimise the design of the quantum dot.
Both purposes require the definition of a Quality-factor (QF). There is no standard definition of the QF, but an appropriate candidate could be defined as the ratio of the energy difference between two potential wells, such as the ones seen on Figure 9, **b**, and the barrier between them.
However, as computers and especially machine-learning algorithms have a tendency to perform their *exact* purpose, and not necessarily the intended one, it is recommended that the QF is defined with care[89].

To aid in this goal, a penalising function could be implemented, which would penalise the algorithm for producing potential wells that are too dissimilar in depth. This would ensure that the algorithm does not simply produce the one extremely deep potential well, but rather six optimal ones.
Similarly, complexity in the resulting field could be penalised, for a currently undefined measure of complexity.

Once the quality factor and the penalising function are defined, two seperate machine-learning algorithms could be implemented. Imagine a nestled for-loop, in which the first algorithm changes a design feature, for which the second algorithm then tunes the gates for an optimal field. Continue until you exhaust the design parameter space, and find the design for which the QF is maximised.

This would be a powerful tool, as it would allow for the optimisation of the quantum dot design, without the need for human intervention, and would allow for the design of quantum dots that are not only optimal but also not necessarily intuitive.

3.3.3 Code Optimisations

As a standard, the library FreeFEM++ used in this work, uses a single core for processing. This is a significant bottleneck, as the simulation is computationally heavy, and could benefit from parallel processing. This would be especially beneficial for the machine-learning algorithm, which needs hundreds, if not thousands of iterations to function properly, as it would significantly decrease the computation time. This would be implemented by using Domain Decomposition Methods (DDM)[90], which would allow for the simulation to be run on multiple cores, also known as parallelism.

4.

Device Fabrication and Experimental Techniques

There are a myriad of techniques and considerations to work through when fabricating micro- and nano-scale devices. In this section, we will outline the fabrication techniques used to create the devices used in this work, the characterisation techniques used to characterise the fabricated devices, as well as the materials used in the devices, the failure modes encountered during fabrication, and how to mitigate them.

4.1 Fabrication Techniques

The fabrication of micro- and nano-scale devices is a delicate process, requiring a high degree of precision, control, and consistency particularly for complex multi-layer devices such as the ones attempted in this thesis. Below is an outline of the various techniques used to achieve this precision, control, and consistency.

4.1.1 Electron Beam Lithography

Electron-Beam Lithography (EBL) utilises a focused beam of electrons to expose a resist on a substrate. The resist is a material that is sensitive to the electrons, and once exposed, it can be developed, i.e., removed, in a developing agent (See Figure 15, **a** - **b**). The resist is used to protect parts of the substrate from the deposition of metal, and to allow for the creation of a pattern on the substrate.

The pattern that is "written" into the resist, is the output of Section 2.5.1, i.e., a computer aided design (CAD) file. By segmenting the design files into different layers, we can control exactly which sections of the design are put down in each step. This allows for the creation of complex, multi-layer devices, such as the ones used in this work.

However, utilising EBL tools (Elionix 125kV) for the creation of complex devices is not without its challenges. First is the question of which resist to use. There is a myriad of resists to choose from, and they all have different characteristics. Some are more sensitive to the electron-beam, i.e., their dosage is lower, some are more resistant to the developing agent, i.e., their developing time is longer, and some are more resistant to etchants such as hydroflouric acid. All vary in thickness. The choice of resist is crucial, as it can make or break the fabrication of a device. A general rule of thumb is to use a resist that is 2-3 times thicker than the metal layer that is to be deposited, as this allows for a good lift-off, a minimum of collapsed side-walls, and a good definition of the structures.

The second challenge is the fine-tuning of the resolution and speed of the exposure. Generally, the higher the resolution, the slower the exposure, as the electron beam is smaller, it takes it longer to cover the same area. For this reason, the designs are split into two main sections: The local structures, which are the finely grained, and the global structures, which are large, where over-exposure and blurred details are inconsequential. The local structures are written with a higher resolution, whereas

the global structures are written with a lower resolution. This provides a balance between the speed of the exposure, and the resolution of the structures.

The third challenge is the alignment of the different layers. Since the device is created in several layers, it is crucial that the different layers are aligned correctly. This is done by using alignment markers, which are used to align the different layers. The alignment markers are placed on the substrate in the first step of the fabrication process, and are used to align every following layer.
There are two types of alignment markers: global and local. More is explained in Section 4.3.1.

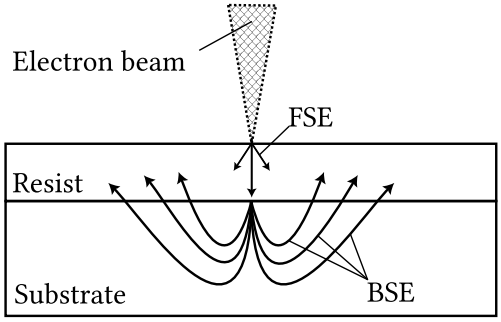

Figure 13:
Proximity Effect

The proximity effect of an electron beam: FSE are forward-scattered electrons, BSE are back-scattered electrons. Adapted from[93]

The fourth challenge is a phenomenon known as the proximity effect[91,92,93] and how to correct for it. As seen on Figure 13 the proximity effect is the scattering of electrons, which causes the electrons to spread out, and thus, the structures are not as well-defined as expected. The main cause of the over- or underexposure are the back-scattered electrons (BSE) which start back-scattering at the substrate-resist interface. However, the forward-scattered electrons (FSE), which are scattered from the vacuum-resist interface, also play a role. There are generally two main classifications of proximity effects: Intraproximity and interproximity. The interproximity effect is concerned with the effect caused by nearby structures or structures whose corners have an angle that follow: $\angle < 180°$, where the angle is defined on the outside of the structure, such that the corner recieves more dosage than the bulk edge of the structure. The intraproximity effect is concerned with the effect caused by corners follow $\angle > 180°$, such that the corner receives less dosage than the bulk edge. This can be corrected for by using a technique known as proximity effect correction (PEC), in which the structure gets segmented into smaller elements, which all receive a specific dosage multiplier, depending on their surroundings.

While the mathematics and details of the PEC are complex and outside the scope of this work, we refer the reader to P. Li[91], J. M. Pavkovich[94] and GenISys[95] for in-depth explanations of the concept of edge-equalisations and the mathematics behind PEC.

The three-layer microchips attempted in this thesis, require a total of 8 EBL rounds, 7 of which require at least global alignment.

4.1.2 Wet-Etching: Hydroflouric Acid and Transene-D

For the ohmic layer and the sub-gate protection ridge, there is a step between developing and depositioning: Etching.

For the ohmic layer, i.e., the gates that are to make ohmic contact with the quantum well, the native oxide of the SiO_2 passivation layer needs to be removed, to allow for the ohmic contacts to anneal through the heterostructure into the quantum well. This is done via a 10-second dip in a 6% Buffered Hydroflouric acid solution[50,96], which removes the native oxide, followed by 10s each in three seperate beakers of millipore water, and a 10 s dip in iso-propanal. The HF is a dangerous acid, and needs to be handled with care, as it can cause severe burns, and is highly toxic. The HF is used in a fume hood, with task-specific gloves, an extra apron, and a visor. The waste is disposed of in a specially designated

container, as it is a hazardous waste.
However, there is also an element of haste associated with the procedure, to ensure that an oxide does not grow back, as a bare SiGe surface is now exposed to the ambient atmosphere[97].

For the buffer stacks, the accumulated Al_3O_2 (alumina) residing on top of the screening/plunger/barrier gates, needs to be removed, for the bonding pads to be exposed, and to create ohmic contact with the buffer stacks. This is done via a Transene-D etch, for 2 minutes and 10 seconds at 50 ℃, which removes approximately 20 nm of alumina. It is followed by a 10 s dip in 50℃ millipore water, and a 10 s dip room-temperature millipore.

4.1.3 Electron Beam Evaporation

Electron-Beam Evaporation makes use of a focused beam of electrons to evaporate a metal onto a substrate. A sketch of the process can be seen on Figure 14. The tools used for these processes are the AJA International ATC-E and the Kurt J. Lesker Electron Gun Chamber. The latter being used supremely for SiO_2 depositioning. An electron beam is focused onto a sample of metal which lies in a crucible, it is evaporated onto the substrate in a directional manner. This allows for the deposition of a thin layer of metal onto the substrate. The metal is deposited in an ultra-high vacuum chamber, which is pumped down to a pressure of ~10^{-6} Torr. Different metals have varying evaporation energies, which require the use of differing electron beam currents, that also control the rate of deposition. The thickness of the metal layer is controlled by the time of deposition.

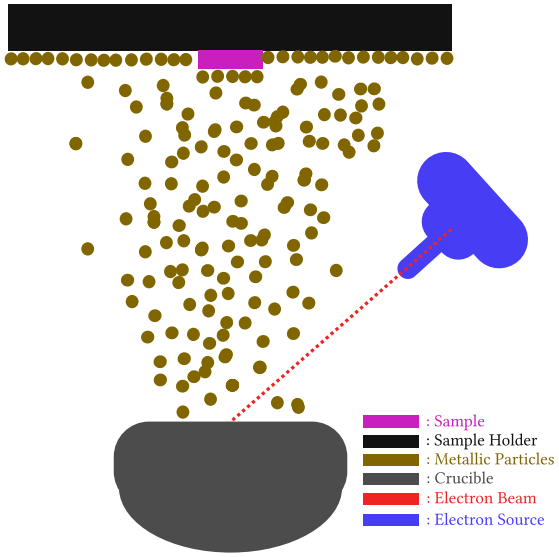

Figure 14:
E-Beam Evaporation

Electron beam evaporation sketch, showcasing the procedure utilised to deposit nano-films onto a substrate using a high-energy electron beam.

After the deposition step, the device is entirely coated with a thin layer of metal. The resist between large parts of the device, and the deposited metal is removed via a lift-off agent (See Figure 15, **c - d**). Common lift-off agents are: 1,3-Dioxilane, Acetone, or N-Methyl-2-Pyrrolidone (NMP), depending on which resist is utilised. After the lift-off, all that remains on the substrate, are the metal structures that were written into the resist.
Following this procedure, there are now bare metal gates on the substrate. The next step is to insulate the metal gates from the next layer of gates. This is done via Atomic Layer Deposition (ALD) of a layer of dielectric material, such as alumina, the dielectric material used in this work.

4.1.4 Atomic Layer Deposition

Since the device has several layers, in which the gates overlap, a dielectric material is needed for electric insulation. This is done via Atomic Layer Deposition (ALD). ALD is a process in which a thin layer of material is deposited onto a substrate, by exposing the substrate to a series of reactive, gaseous substances, such as H_2O and trimethylaluminium ($Al(CH_3)_3$)[98], which react to form an extremely uniform dielectric. The process is repeated until the desired thickness is achieved. The thickness of the layer is controlled by the number of cycles, i.e., the number of times the substrate is exposed to the gaseous substances.

The ALD process is done in a chamber, which is pumped down to a pressure of ~10^{-6} Torr, while the chamber plate/substrate is heated to a temperature of ~150 °C.

For our purpose, Al_2O_3 was chosen as the dielectric due to its high dielectric constant, $\kappa = 9$, and low leakage current density[99], which allows for an approximate oxide thickness of ~7 nm, enough to insulate the metal gates, while still allowing a workable lever-arm on the 2-DHG.

The full-cycle precursor reaction can be written as follows[100]:

$$2Al(CH_3)_3(g) + 3H_2O(g) \rightarrow Al_2O_3(s) + 6CH_4(g) \tag{4.1}$$

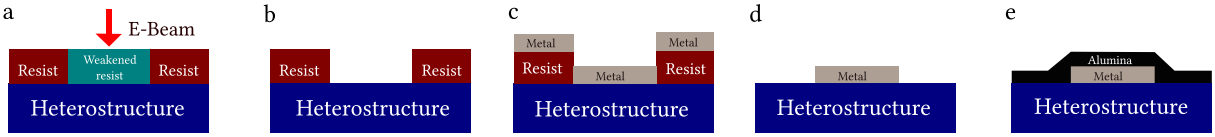

Figure 15 Sketch of a round of EBL followed by ALD. **a**: Electron beam exposing a part of the resist. **b**: Resist stack following developement. **c**: Post depositioning of a metal using electron beam evaporation. **d**: Following lift-off. **e**: Following a deposition of Alumina in the ALD procedure.

The full ALD cycle also plays another role in this fabrication: annealing.

4.1.5 Annealing

Following the wet-etching of the native SiO_2 passivation cap and placement of the ohmics, the device is annealed. Annealing is a process in which the device is heated to a high temperature, to allow the ohmic contacts to diffuse through the substrate into the quantum well. This is done to create a low-resistance contact between the ohmic contacts and the quantum well. The annealing is done in the ALD chamber, as it allows for a high vacuum and high temperature environment. A consideration to make for the annealing temperature, is the thermal budget for the heterostructure, i.e., when does the strained Germanium layer relax. The thermal budget for the heterostructure is ~400 °C[101].

The annealing is incorporated into the ALD cycle, as a pre-step to the depositioning. The device is heated to a temperature of ~250 °C, and held there for 2 ½ hours. This allows for the ohmic contacts to diffuse into the quantum well, and create a low-resistance contact.

4.2 Characterisation Techniques

During or after the fabrication of devices, it is often critical to be able to characterise their physical properties. In this sub-section we will outline the characterisation techniques used in this work, and how they were used to characterise the devices.

4.2.1 Scanning Electron Microscopy

While a full discussion of how a scanning electron microscope functions, is out of the scope of this work, a brief overview will be given here. For further information, the reader is referred to W. Zhou[102] and A. V. Girão[103].

Scanning Electron Microscopy (SEM) is the use of scattering electrons instead of photons to create an image. This advantage of utilising electrons, is that they are not limited by the diffraction limit of light[102], and can thus create images with a much higher resolution.
Throughout this work, two primary sources of electron signals are used[103]: secondary electrons and back-scattered electrons.

Secondary electrons are electrons that are ejected from the material due to ionisation via the electron beam. These are usually fairly low in energy, 3-5 eV, and thus only provide information about the first few nanometers of the material. This causes them to be able to give topological information with high resolution. This is the signal used for general imaging.

Back-scattered electrons are electrons from the electron beam, that are back-scattered via a single or multiple scattering events. They are scattered by elastic collision with the specimen atomic nucleus, and their energy is on the order of 50 eV. Because of this, a higher atomic number material, will cause a higher back-scatter signal. This allows for the creation of images with a high contrast, as more massive atoms have a larger interaction cross-section. The back-scattered signal is generally used for the location of markers, due to the markers having a high atomic-number material, such as gold or platinum. This allows for an excellent contrast between a substrate made of silicon and germanium, and the markers made of gold or platinum.

4.2.2 Energy-Dispersive X-Ray Spectroscopy

Energy-dispersive X-ray spectroscopy (EDX) is a technique in which the ionisation and consequent X-ray emission of a material is utilised to determine the elemental composition of said material.

In combination with the SEM, we can allow an incident electron-beam to ionise a material, whereby electrons in tightly bound inner states are ejected, and electrons from higher energy states fall down to fill the state. This causes the emission of X-rays, which are characteristic of the element. By measuring the energy of the X-rays and the count-per-second (cps), the elemental composition of the material can be determined.

4.2.3 Spectroscopic Ellipsometry

Spectroscopic ellipsometry (SE) utilises the interaction between linearly polarised light and an ambient medium, a thin film, the substrate, and previous knowledge of a sample, to derive a thin-film thickness[104].
In this work, it was utilised to ascertain the film thickness of ALD-deposited alumina. The thickness of the alumina layer is crucial, as it needs to be thick enough to insulate the metal gates, but thin enough to allow for the metal gates to maintain a workable lever-arm.

4.2.4 Leakage Matrix Diagnostics

Leakage matrix diagnostics is a characterisation technique, in which the resistance between various gates is measured, to ensure that there are neither short-circuits between the gates nor that the gates are leaking to the substrate. This is done by applying a bias voltage between a set of two gates, measuring the current that flows between the gates, and calculating the resistance. This is done for all possible combinations of gates, to ensure that there are no short-circuits or leakage currents between the gates. This is crucial, as a short-circuit or leakage current can render a device non-functional.

There are three main failure modes that can be detected during the leakage matrix diagnosis:
1: Short-circuits between neighbouring intralayer gates: This indicates a fabrication issue, in which the gates are either overexposed, or the design needs to change.
2: Leakage currents between neighbouring interlayer gates. This indicates an ALD issue, in which the dielectric layer is not thick enough, or it is not sufficiently uniform.
3: Leakage currents between non-neighbouring inter- or intralayer gates. This indicates a substrate leakage issue, in which the metal gates are not properly insulated from the substrate. This is usually caused by a puncture during the bonding process, as mentioned in Section 4.5.1.

The temperature at which the matrix is taken is crucial, as the third failure mode cannot be detected at base temperature (~12 mK), where the substrate has frozen out all charge carriers. Therefore, it is usually taken at room temperature, and again at base temperature.

To ease the leakage matrix diagnosis, an automated script was written. The script utilises the naming scheme from the simulation, assigns each gate with the appropriate number of neighbours (only for gates in the same layer), based on a pre-defined max-distance, and also assigns each gate with an overlapping area, based on the overlap between the gates. By then defining a set of rules, and a leakage limit, it assigns each value in the leakage matrix, above the leakage limit, a value based on which failure mode it is most likely to be. This allows for a quick and easy diagnosis of the leakage matrix, and a quick identification of the failure mode. The set of rules is as follows:

Rule no.	**Definition**
No. 0	If the value between two gates is below the leakage limit, then there is leakage between them.
No. 1	If there is a leakage between two gates, and they are both neighbours, then the leakage mode is an intralayer failure.
No. 2	If there is a leakage between two gates, and they are not neighbours, but they overlap, then the leakage mode is an interlayer failure.
No. 3	If there is a leakage between two gates, and they are neither neighbours nor overlapping, but the leakage is to an ohmic, then it is a substrate leakage failure.
No. 4	If none of the above apply, then it is an unknown failure.
No. 5	Iterate through all gates again: If two gates have an unknown failure mode, but each also leak to an ohmic, then it's substrate leakage.

Table 3: Leakage Matrix Rules

The rules, which the automated script follows, to assigns each leakage to a specific failure mode.

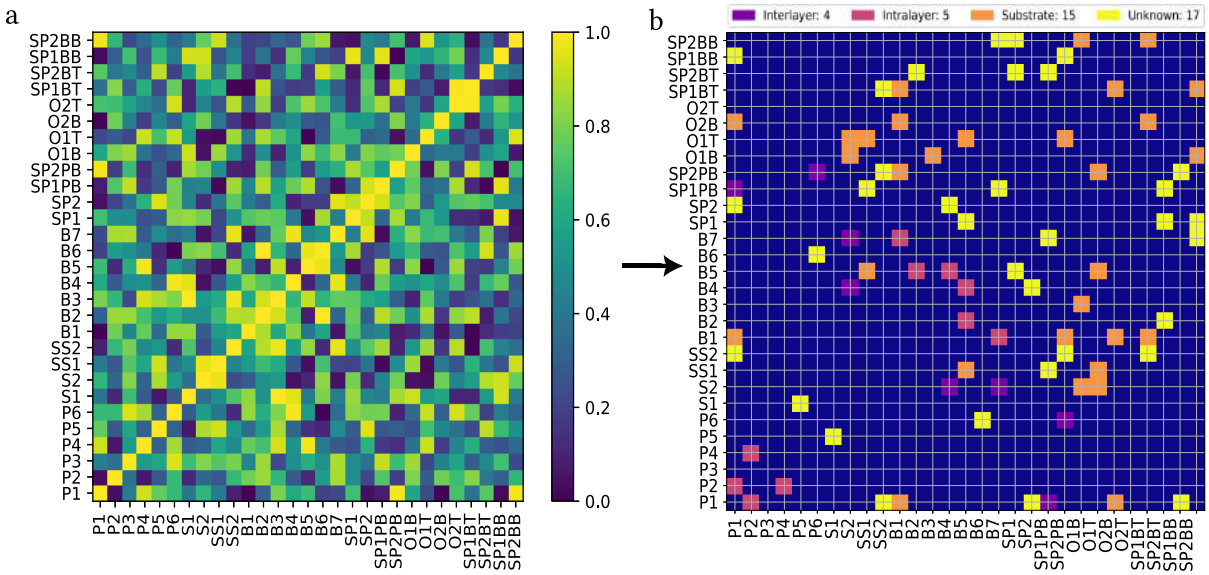

Figure 16 **a**: A randomly generated, normalised leakage matrix, symmetric around the diagonal, for the device shown in Figure 8, **c**. **b**: The analysed leakage matrix, showing the various types of failure modes, which can be detected by the leakage matrix diagnosis.

These rules are simplistic, and they do not take into account the possibility of a leakage, which it assigns to be an intralayer failure, to actually be a substrate failure. However, if the leakage matrix is taken at both base- and room temperature, this issue should vanish.

Figure Figure 16 showcases the leakage matrix diagnosis, and the various failure modes that can be detected by the leakage matrix diagnosis. The figure shows a randomly generated, normalised leakage matrix, symmetric around the diagonal, for the device shown in Figure 8, **c**. The analysed leakage matrix, showing the various types of failure modes, which can be detected by the leakage matrix diagnosis, is shown in **b**. The alpha-numerical codes for the gates, can be found in the appendix.

Unfortunately, this diagnostics tool was never fully utilised, due to unfortunate circumstances with the data acquisition, however, it could be a useful tool if utilised in future work.

It should be noted that for a real device, no leakages should occur as unknown.

4.3 Material Considerations and Device Structure

Generally, noble metals such as gold, platinum, and palladium are used in the fabrication of micro- and nano-scale devices, due to their high conductivity, and generally inert nature. This makes them ideal for use in devices, as they do not react with the environment, and do not degrade over time.
However, their inert nature and low chemical reactivity is a double-edged sword, as they are difficult to adhere to semi-conductor substrates, as most substrates readily form native oxide caps, which can cause them to degrade over time, as their adhesion weakens. To combat this, a 5nm titanium adhesion layer is used, which creates a stronger adhesion of the gates to the substrates[105,106,107], since titanium more readily reacts with the oxide layer of the substrate, than the platenoids and gold.
Thus, all layers of the device, except for the ohmic gates, have a 5nm titanium adhesion layer.

The various material considerations made for each layer are considered below, in order of deposition.

4.3.1 Alignment Markers

Global alignment markers are placed on outer edges of the chip design, and are used for a rough alignment of the different layers. Local alignment markers are placed much closer to the center of the design, but a minimum of 120 μm away from inner structures, to ensure that the inner structures do not get overexposed from the search algorithm of the markers. These are used for a much finer alignment, and can ensure inter-layer alignment of less than 10 nm.

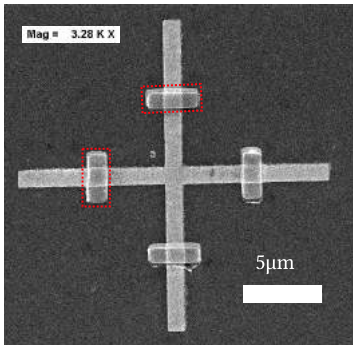

Figure 17: Marker Degredation

Local Marker degredation, two of them outlined by a dashed, red line, caused by the autosearch function of the EBL.

Another consideration to make regarding the alignment markers, is the choice of metal. The metal used for the alignment markers needs to be a high-contrast metal, such as gold or platinum, as the alignment markers need to be visible, both initially and ultimately, in the scanning electron microscope (SEM), over the course of many layers. The SEM can cause degredation in the metal and in the contrast of the metal, so a high-contrast metal is needed. Not only can the SEM cause degredation, but the metal of choice also needs to have a high diffusion temperature, so that they do not deform, as the metal will be exposed to high temperatures during the annealing process. A usual choice of metal is gold, however, platinum is also a viable choice. This work

utilised gold, as it is easier to work with, and while the diffusion temperature is lower than that of platinum, it is still high enough to withstand deformation during the aluminium annealing.

A thickness of 50 nm was chosen for the alignment markers, as this thickness allows for a good contrast in the SEM and issue-free lift-off, while using the resist CSAR13.

4.3.2 Ohmic Contacts

The ohmic contacts are used as a source and a drain, i.e., to populate the quantum dots, for the quantum well in the heterostructure. Aluminium was chosen due to its material properties as a soft superconductor[108,109] , meaning the critical field strength is low, and due to it's previous success in similar devices[70,24] .

Extensive testing was done to find the optimal thickness of the aluminium layer, as aluminium is known to adhere extremely well to various surfaces and is difficult to lift-off properly. The optimal thickness was found to be 22 nm, while using the resist PMMA A4, as it allowed for an easy lift-off, and good ohmic contact.

4.3.3 Sub-Gate Protection Ridge

The sub-gate protection ridge is implemented to act as a barrier between the metal gates and the substrate, to prevent a short-circuit between the gates and the substrate.

The main material requirements of the protection ridge are that it is a good insulator, with few defects, and a high melting/diffusion temperature. Silicon-dioxide, SiO_2, was chosen, as it possesses all these qualities, and since it is the same material used for the passivation cap, it is ideal. The thickness of the layer was chosen to be 180 nm, as this thickness allows for a good protection of the bonding pads, while still allowing the metal gates to climb up the ridge.

4.3.4 Screening, Plunger, and Barrier Gates

The screening, plunger, and barrier gates are used to create, pinch-off, and control the potential in the quantum well, thusly creating the quantum dots. The screening gates are used to confine the potential in the quantum well to the circular region created by the lollipop-shaped plunger gates. The barrier gates are used to define the barrier potential and thereby the tunneling rate from dot to dot, and from the ohmics to the dots.

As there is a lot of overlap between the layers, as seen from Section 2.5.1, a consideration to make, is to make each successive layer of metal thicker, such that they can climb up the previous layer. This is done by increasing the thickness of the metal layer by 6 nm for each layer, starting at 22 nm for the screening gates, and ending at 34 nm for the barrier gates.

The chosen metal for the gates is palladium, due to its high conductivity, and its inert nature. Palladium is known to be a good conductor, and is used in similar devices[50,70,24,110] .

4.3.5 Buffer stacks

The buffer stacks are used as a shock-absorbent, to prevent the bonding wire from puncturing through the gates to the substrate, thereby causing substrate leakage, during the bonding process[50].

The buffer stacks are made up of alternating layers of titanium and aluminium. The titanium is used for its adhesive properties, and its relatively high Young's modulus and tensile strength[87], compared to aluminium.

Aluminium is used as it is the same metal used in the bonding wire, meaning it creates a solid bond. It is also used for its relatively low Young's modulus and tensile strength, compared to titanium, as it allows for the buffer stacks to absorb the shock of the bonding process, by allowing the aluminium to deform, while the titanium remains semi-rigid.

4.4 Process Parameters and Results

Having introduced the various materials and techniques used in the fabrication of the devices, we will now discuss the various parameters used in the fabrication of the devices, how they were arrived at, and the results of the fabrication process.

4.4.1 Dose-Testing

The first step is to perform a dose-test, i.e., a test where identical patterns with identical resists, get exposed with various dosages. The aim of this test is to ensure that selected dose does not over- or underexpose the crucial inner features.

Figure 18 showcases the data analysis used to estimate the optimal dose for a specific resist and design. It displays the relationship between a specific feature on **a**: an ohmic, **b**: a plunger gate and the dosage used for the dose-test.
Violin and box plots were chosen to ensure that possible biases in the sample data would be visible. If all data points at a given dosage, came from the same sampling distribution, then the violin plot's kernel density estimation (KDE) should show a Gaussian. However, if data are not pulled from the same sample distribution or the sample distribution is polymodal, this would show up as several different peaks in the KDE. This would indicate that the data is biased, and that either, the dosage is not optimal or there are other phenomena at play, which are not accounted for.

The optimal dosage is the intersection between the linear fit and the design feature width. Of course, a dosage cannot be chosen simply from this, as these data only take into consideration a single feature width, and not the entire design, meaning an informed opinion and inspection of the whole structure is still crucial. However, it is a good starting point, and can be used to estimate the optimal dosage for the entire design.

Figure 19 demonstrates the results of the various layers, along with Figure 23, using the parameters ultimately decided on via the dose-testing process. High resolution, well-defined structures are visible, while being well aligned, visible on **d**.

It is important to note, that Figure 19, **d**, showcases the device used for transport measurements in Section 5.2.2, however, the device suffers from the failure mode mentioned in Section 4.5.5, and is therefore not fully functional.

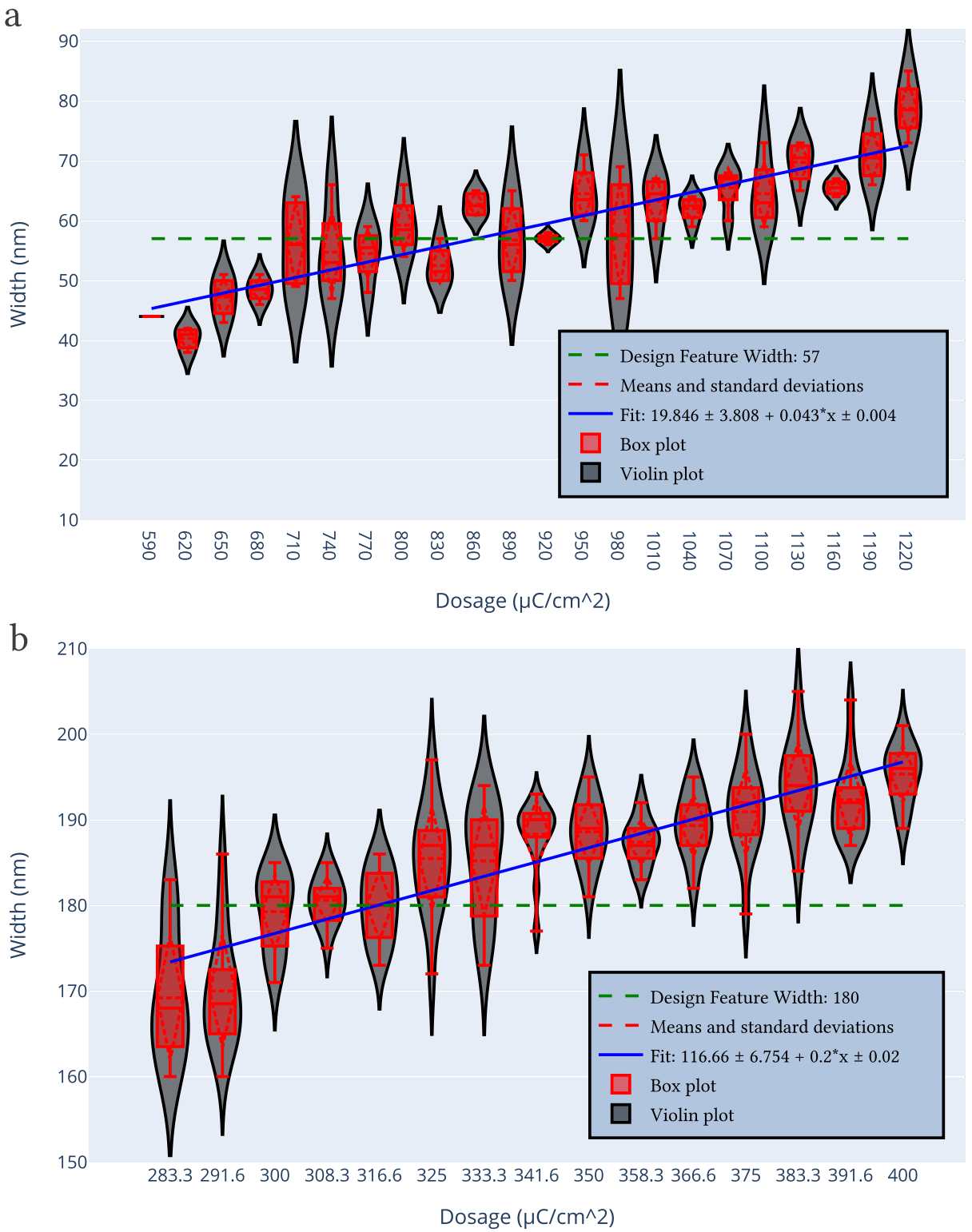

Figure 18 Violin/Box plots of the dose-tests. x-axis: Dosage in $\frac{\mu C}{cm^2}$. y-axis: Width of measured feature in nanometers. A violin plot was chosen to ensure possible biases in the sample data, such as a bimodal distribution arising from bad width sampling, would be visible. The optimal dosage is the intersection between the linear fit and the design feature width. **a**: A test of the ohmic structures using the resist PMMA A2. **b**: A test of the plunger structures, using CSAR4.

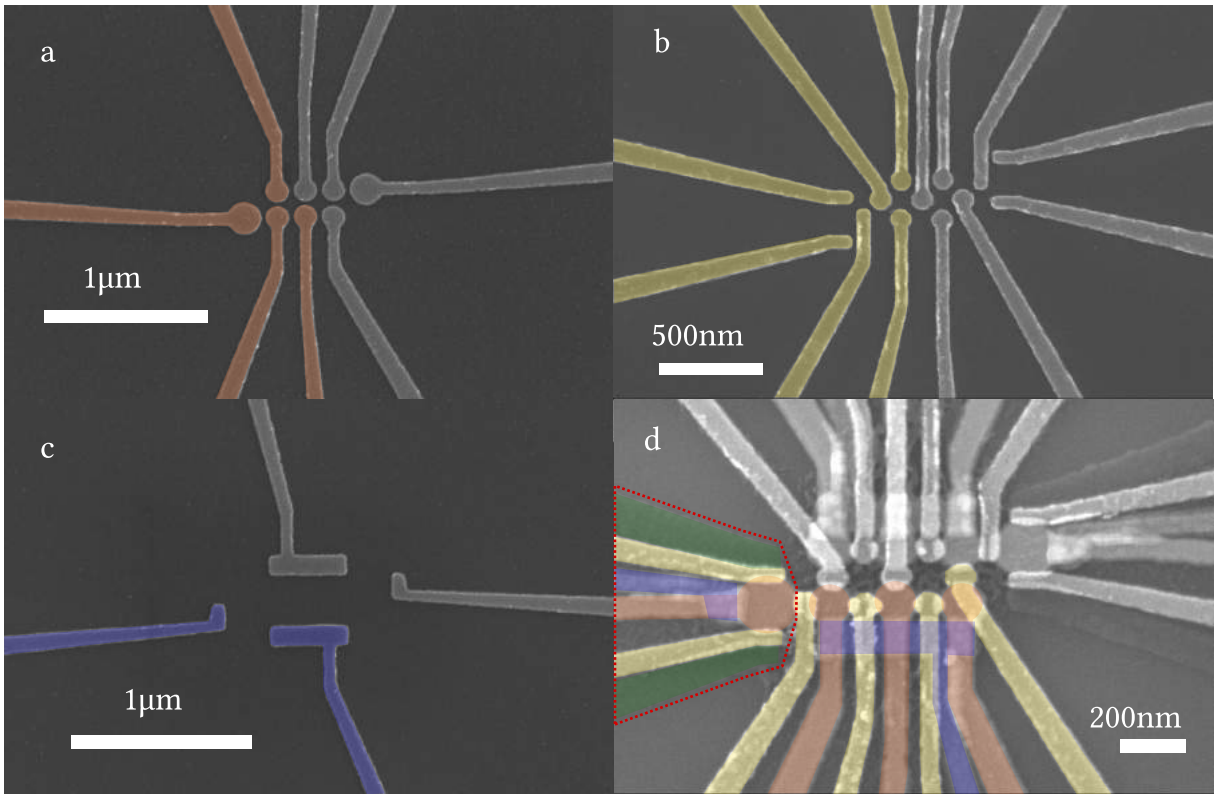

Figure 19 SEM images with final EBL parameters. **a**: Half-false-coloured plunger layer. **b**: Half-false-coloured barrier layer. **c**: Half-false-coloured screening layer. **d**: Half overlaid fully finished design, featuring ohmics (green). Red-dashed outline showcases the quantum dot configuration used in DC measurements in Section 5.2.2

4.5 Failure Modes

The fabrication of complex, multi-layer devices is a delicate process and as such there are a multitude of failure modes that can occur. Throughout the work, we have encountered several of these failure modes, and have developed strategies to mitigate them.

4.5.1 Substrate Leakage

Substrate leakage is a failure mode that occurs when the metal layers of the device are not properly insulated from the substrate. This occurs chiefly due to bond puncturing.

Bond puncturing occurs as a finished device is being bonded to a daughterboard, usually via the F&S Autobonder, and the bond punctures through the metal gate, and into the substrate. This causes a short-circuit between the gate and the substrate, and renders the device useless. Substrate leakage is a monumental issue, as the source-drain voltages are usually on the order of $1 - 5$ mV, whereas top-gate voltages usually range in $300 - 2000$ mV range. This disparity in voltages, results in large currents flowing into the top gates, if they are in contact with the quantum well. To combat this, two safe-guards have been implemented.

The first safeguard is the use of a 180nm silicon-dioxide layer, which is nestled underneath the bonding pads of the metal gates. To ensure that metal gates can climb up this protection stack, a ridge is made on the edge of the SiO_2. To achieve this, an 800nm tri-layer stack of PMMA is used. The resist stack is engineered, such that the two lower coatings have a much lower clearing-dose than the top layer. This allows for the creation of an undercut. As can be seen on Figure 20, **a**, the undercut functions as

an aperture, letting a small amount of the depositioning material through, outside of the aperture's range, and creating a ridge.

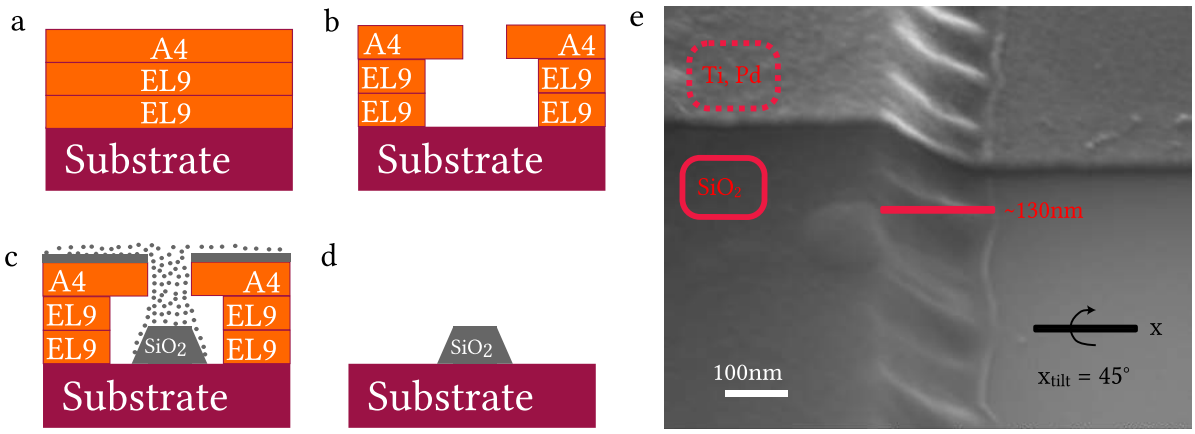

Figure 20 **a**: Tri-layer resist stack of EL9, EL9, and A4. **b**: The undercut created by the resist stack. **c**: Depositioning of the SiO_2 layer. **d**: The SiO_2 left after lift-off. **e**: A SEM image of the SiO_2 ridge, accompanied by a 5 nm Ti/22 nm Pd gate climbing up the ridge.

Figure 20, **b**, is a SEM image of the 180 nm SiO_2 ridge, tilted by 45° around the x-axis, with a ridge baseline of approximately 130 nm. This provides an inclination angle of $\angle_{inc} = 54°$. The figure also shows a metallic gate, consisting of a 5 nm titanium adhesion layer, and a 22 nm palladium layer. The ridge is clearly visible, and the palladium gate is seen to climb up the ridge, without any visual break. This is a clear indication that the ridge is functioning as intended.

The second safe-guard is the creation of buffer stacks; alternating layers of titanium and aluminium deposition on top of the metallic gates, meant to act as a shock-absorber.

These buffer stacks are fabricated by etching any aluminium-oxide from the surface of the metallic gates, and then depositing 50 nm titanium, 100 nm aluminium, and 50 nm titanium, finishing off with 50 nm aluminium.

Later DC measurements (See Section 5.1.1 and Section 5.2.1) confirmed that gates produced with these safe-guards did not leak to substrate.

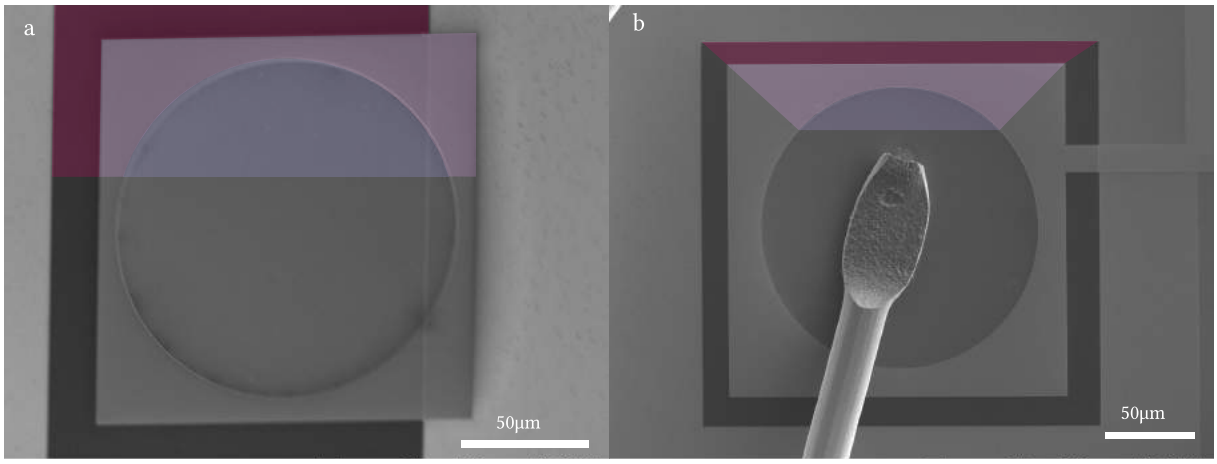

Figure 21 Semi-false coloured SEM images of: **a**: A buffer stack, overlapping with the SiO_2 ridge. **b**: A bonded buffer stack. Purple: SiO_2. Magenta: Titanium/Palladium. Lavender: Buffer stack.

4.5.2 Hydroflouric Acid

Hydroflouric acid (HF) is used to wet-etch the SiO_2 passivation layer[50,96], to allow for the annealing of the ohmic contacts. However, the acid can also delaminate the resists, and cause the metal to lift-off poorly. Figure 22 shows this delamination behaviour. The top image shows an optical image of the bonding pad, where the actual gate outline is defined by a dashed, red line. The bottom image shows a SEM image of the inner structure of the ohmics. The delamination is clearly visible, and the ohmics are not well defined.

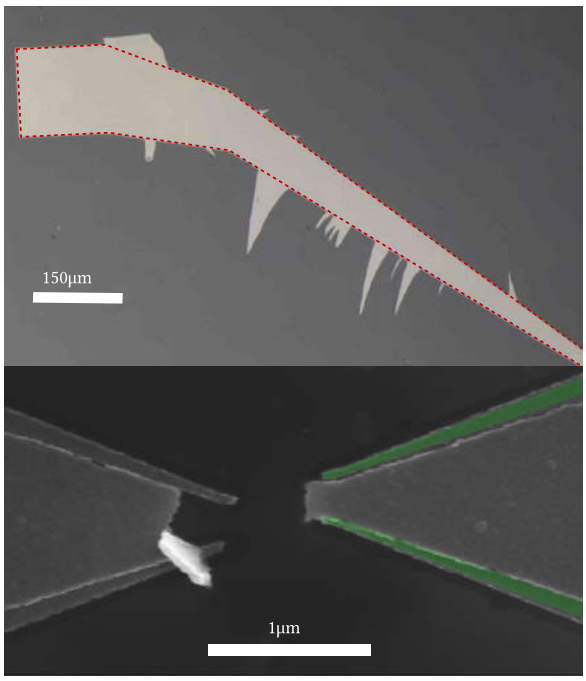

Figure 22: HF-delamination.

Top: An optical image of an ohmic bonding pad/fan-out, post depositioning and lift-off. Resist: CSAR4. **Bottom**: A SEM image of the inner structure of the ohmics, post depositioning and lift-off. Design features overlaid on the right pair. Resist: CSAR4.

This issue was initally thought to be an aluminium issue, as aluminium is known to be a difficult metal to lift off properly, so the initial solution was to decrease the thickness of the aluminium layer. However, this did not solve the issue, although it did partly alleviate it.

The CSAR resist line is known to be weak to HF[50], so a suggestion was to switch to a different resist line, PMMA.

However, issues still persisted, and the final solution was to decrease the aluminium gate stack to 22 nm, switch to PMMA A4, pre-bake the resist for 20 s at 100 ℃ to allow for reflowing, and to decrease the developing time to 45 s from 60 s. This allows the resist profile to reflow from a undercut-like profile into a ridge-like profile, lessening the risk of HF flowing underneath the resist and causing delamination.

This recipe yielded a significantly higher success rate.

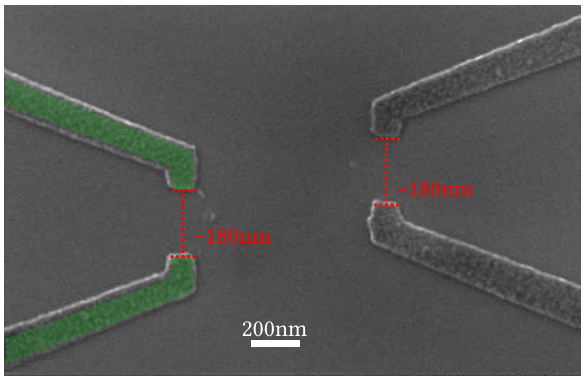

Figure 23: Well-defined Ohmics.

SEM image of a well-defined ohmic gate, pre-annealing, with the design features overlaid on the left pair.

Figure 23 is a SEM image of a well-defined ohmic gate, pre-annealing. The gate is generally well-defined, has a slight overexposure, as defined by the overlaid design features, and has a clear outline. This is a stark contrast to the delaminated ohmics, as seen in Figure 22. **Note**: The ohmics designs on Figure 22 and Figure 23 are not identical, as later rounds of fabrication added the slight L-shape. The distance between the ohmic contacts is measured to be true to design, 180 nm.

4.5.3 Misalignment

There are three main forms of misalignment: Interlayer misalignment, stitching errors, and current-switching misalignment. All three can cause havock and render devices unusable. Interlayer alignment stems from either poor alignment to global and/or local markers or combined drift in the electron coloumn and stage. Stitching errors occur when there's significant drift during an exposure. Current-switching misalignment occurs when there's significant drift during the wait time, while switching beam currents. Misalignment can cause a multitude of issues, such as short-circuits or floating gates, and can render a device useless.

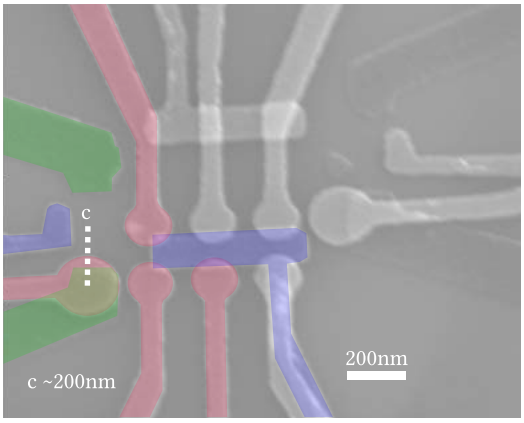

Figure 24: Interlayer Misalignment

Half-false-coloured SEM image of interlayer misalignment. Screening and ohmics gates are well-aligned, however, the plunger gates are misaligned with the remaining layers by approximately 200 nm.

Figure 24 showcases interlayer misalignment by approximately 200 nm. As is evident, this device would have been non-functional, as the plungers are completely misplaced with regard to their intended position, and would therefore not function as intended. This type of misalignment occurs when the global and/or local markers are not properly aligned, or when there's drift in the electron coloumn and stage.
Figure 25, **a**, **b**, **c**, showcases stitching errors between structures in the same Beamer file, with the same electron-beam current, and an identical dosage. The exactly matching pieces, that are both clearly developed, leads us to believe that this is in fact misalignment between write-fields in the Beamer file. Beamer splits the full lithography profile into smaller write-fields, meaning that certain parts of continuous structures are not written in succession to the rest of the structure.

A sketch of this can be seen on Figure 25, **d**. Numbers indicate the order the write-field is written in. Following this patterns means that section 3 and 5 of structure B are not written in succession, and can therefore be misaligned, if there is drift in the system.

As can be seen on Figure 26, there is significant drift in both the 125kV Elionix and the 100kV Elionix tools. The initial tool used for this thesis was the 100kV Elionix system, however, after experiencing significant misalignment issues, the tool was switched to the 125kV Elionix system. While this did improve the alignment, as shown on Figure 26, **a**, there is still significant drift in that system. The drift in the system can be seen to increase exponentially, during the first 25 minutes after loading, but reaches a linear regime with the total drift being approximately 200 nm. For this reason, it is recommended that users of the tool, waits at least 25 minutes following the loading of the sample, before use.

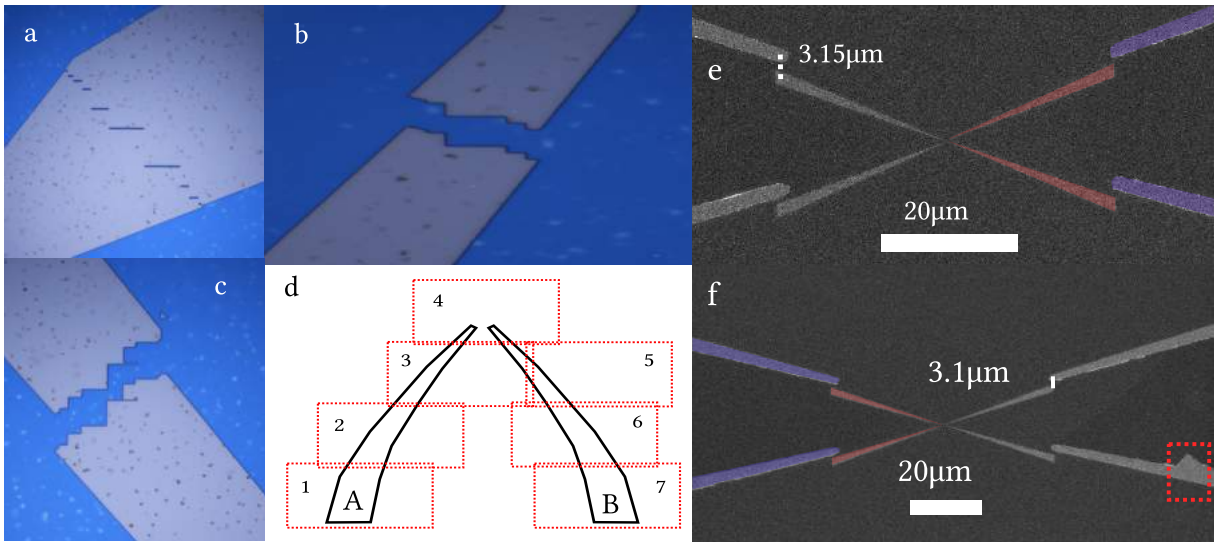

Figure 25 **a**, **b**, **c**, Optical images of developed CSAR4 resist. Misalignment in between write fields of the electron-beam lithography is visible. **d**: Sketch of write-field write succession. **e**: Half-false coloured SEM image of current-switching misalignment between inner and outer structures **f**: Half-false coloured SEM image of current-switching misalignment between inner and outer structures. An HF-delimination can also be seen in the red outline.

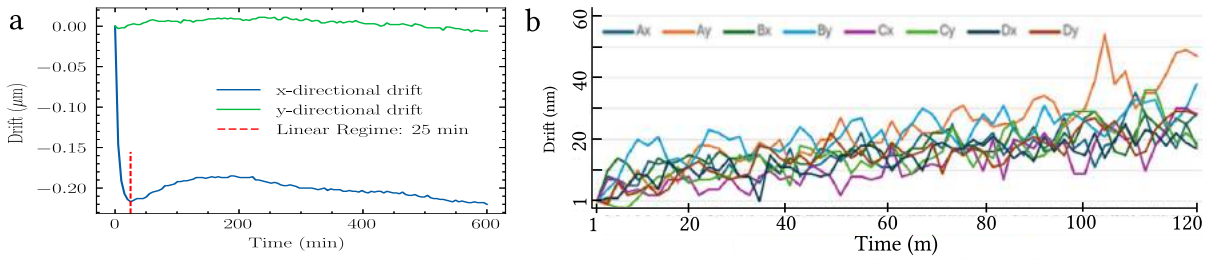

Figure 26 **a**: Combined column and stage drift as a function of time, in the Elionix 125kV system, with a 300 second interval. **b**: x- and y-directional drift, measured at 4 different markers, A, B, C, and D, in the 100kV Elionix System, with a 120 second interval. Data courtesy of the Niels Bohr Institute Cleanroom staff.

4.5.4 Proximity Effect Correction Induced Underexposure

For all gates, a PEC scheme was utilised to correct for the proximity effect. However, the PEC scheme was not perfect, and caused underexposure for a specific region of the inner ohmic structures.

As can be seen on Figure 27, **a**, the underexposed resist is clearly visible in high contrast compared to the metal surroundings, and the metal gate is not well defined. It aligns well with the lower dosage segments of the PEC scheme. The overlapping area between the inner and out ohmics is well defined, as the area was exposed twice.

While there does not actually seem to be a break in the metal gate, as confirmed by later measurements, the underexposure is still a significant issue, as it can cause floating gates, non-operational ohmics, and render the device non-functional.

This is prime example of the edge-equalisation reaching a clearing dose, whereas the bulk of the structure does not. This is a common issue with PEC schemes, in which the correction over-corrects, and assumes the bulk will receive too high of a dose. It can be mitigated with various techniques, such as increasing the base dosage, which could affect the accuracy of fine structures, or by redesigning the geometry of the structures, to accomodate for the underexposure, i.e., make the structures thinner where the PEC causes underexposure.

As seen on Figure 27, **b**, the underexposure issue was solved by redesigning the inner ohmic structure, such that the arm was made thinner. This allowed for the PEC segmentation to not cause underexposure, and the inner ohmic structure was well defined.

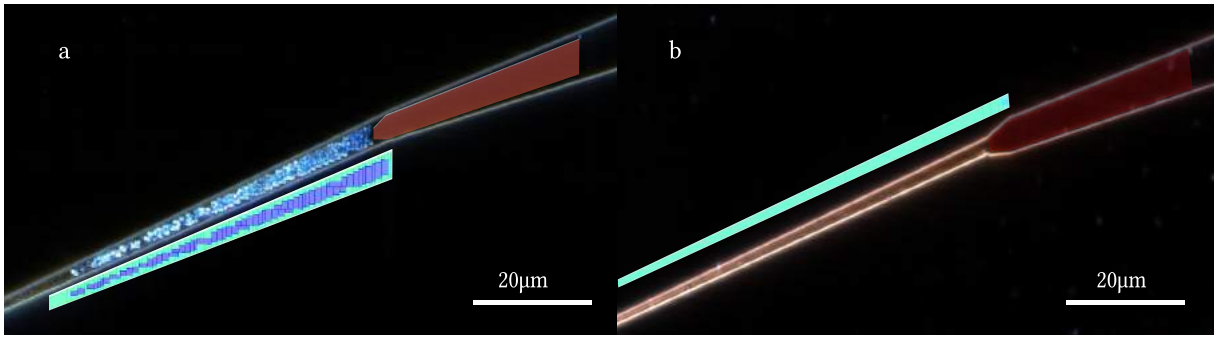

Figure 27 **a**: Optical dark field image on an arm of the inner ohmic structure, showcasing underexposure. The layer is finished, so metal has been deposited. The underexposed resist used for this run, shows up in high contrast compared to the surrounding metal, since it was never developed. Underneath the arm, are the design features, showcasing the segmented PEC scheme. Green signifies a higher dosage multiplier, while blue is lower. The lower dosage segments align well with the seen high contrast regions. Overlaid on the arm, is a the outer ohmic design feature. As can be seen, where the outer ohmics are overlaping with the inner ohmics, the underexposure is non-existant, as the area was exposed twice. **b**: Optical dark field image of the solution to the underexposure issue. The inner ohmic structure has been redesigned to accomodate for the underexposure. The arm has been made thinner, such that the segmentation does not cause underexposure.

4.5.5 Palladium Peel-Off

During one of the fabricational runs, a previously unknown failure mode was discovered: Palladium peel-off. This failure mode occurs when the palladium layer is not properly adhered to the titanium adhesion layer, and can cause the palladium layer to peel off. This causes the gate electrodes to be poorly defined, and renders the device non-functional.

Seen on Figure 28, **a**, is a SEM image of two fully peeled-off palladium gates, post lift-off. An example of an unaffected gate, is outlined in black, while a peeled-off gate is outlined in red. The titanium adhesion layer is clearly visible, which is confirmed by the EDX spectrum, seen on Figure 28, **b**. The EDX spectrum shows a weak peak for titanium, which is to be expected, as it only contains 5nm, and no peak for palladium, which should have a much stronger peak if the full 28nm were present.

The true cause of this issue was never discovered, however, there are few remedies that can be taken to mitigate this issue. The first is to ensure a stable depositioning rate, when depositing the palladium, as unstable rates can cause a fluctuating grain size of the palladium, leading to non-uniform depositions. The second is to ensure a sufficiently full palladium target, as a near-empty target can cause fluctuating

depositioning rates. The final remedy is to allow the lift-off agent to work passively for 2 hours, before actively attempting lift-off with a pipette, as can be seen in Section 7.1.

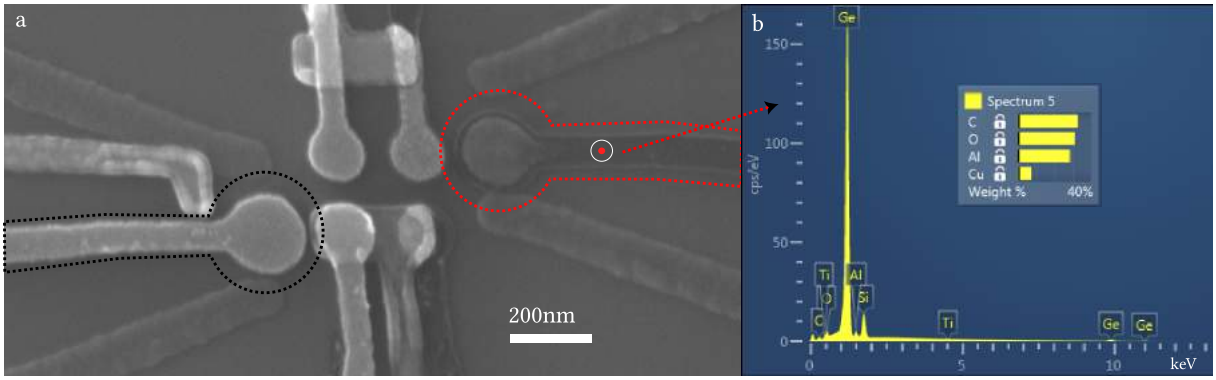

Figure 28 **a**: SEM image of two peeled-off palladium gates, post lift-off. Black outline: Palladium gates. Outlined in red: The peeled-off palladium, with an outline of titanium visible. **b**: EDX spectrum, showcasing a presence of titanium, and an absence of palladium.

4.5.6 Atomic Layer Deposition Pump Failure

During the fabrication of the devices, a "pump failure" occured. This event refers to the loss of a chip during the ALD process, either due to an anomalously large, sudden pressure increase in the chamber during a pump of precursor, or due to a sudden pressure change during the pump-down or release of vacuum. This can cause the device to be lost, as the pressure change can cause the device to be ejected into the pump-line. In order to mitigate this, two sites were designated as A and B, where the real chip and the dummy chip are placed respectively.

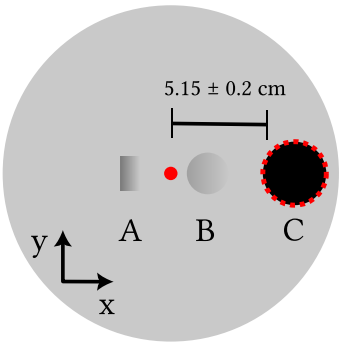

Figure 29: ALD Layout

Top-view of the ALD chamber, with the two designated sites, A and B, marked, with the chip and dummy chip, respectively. C is the pump-hole.

To test the displacement due to this phenomenon, 9 rounds of ALD was deposited in this configuration, where the displacement of both the real and dummy chip was measured. The results of these measurements can be seen on Figure 30, **a** and **b**, which show that chips placed on site A, has an average displacement of: $\overline{\Delta A_x} = 0.14 \pm 0.04$ cm and $\overline{\Delta A_y} = 0.02 \pm 0.02$ cm, whereas chips placed on site B has an average displacement of $\overline{\Delta B_x} = 3.31 \pm 0.11$ cm and $\overline{\Delta B_y} = 0.33 \pm 0.07$ cm. The generally large displacement in the x-direction and low displacement in the y-direction showcases the risk of a chip being ejected into the pump-line, as the displacement is large enough to cause a chip to be ejected.

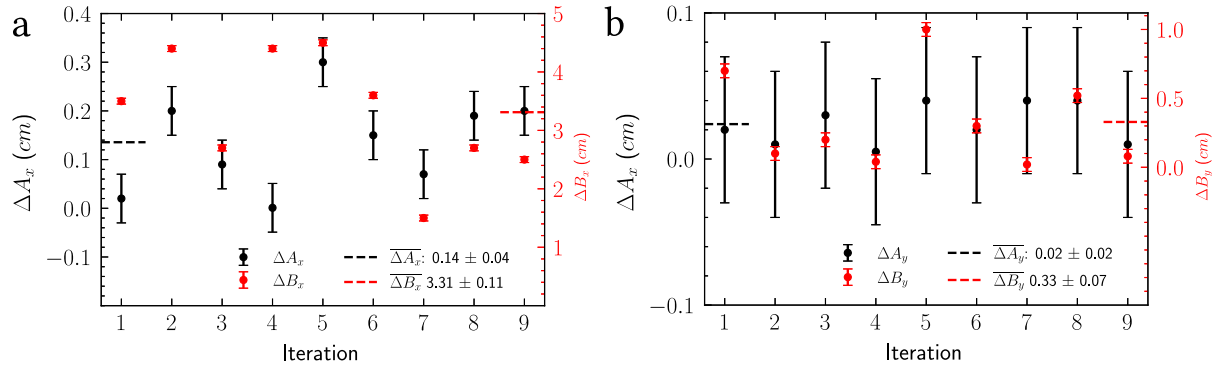

Figure 30 **a**: x-directional displacements of chips placed on site A and B. **b**: y-directional displacements of chips placed on site A and B.

4.6 Refrigeration Techniques

The sub-Kelvin experiments in this work were performed using two different types of refrigeration techniques: dilution refrigeration and adiabatic demagnetisation refrigeration (ADR). The dilution refrigeration technique[111] is based on the mixing of two isotopes of helium, ^{3}He and ^{4}He. The adiabatic demagnetisation refrigeration technique[111] is based on a paramagnetic salt, which is magnetised, followed by adiabatic demagnetisation to allow the salt to absorb heat from the sample. Both techniques require low initial temperatures to function, and are pre-cooled by a pulse-tube refrigerator.

4.6.1 Dilution Refrigeration

The dilution refrigeration technique is based on the mixing of two isotopes of Helium, ^{3}He and ^{4}He. ^{4}He has a nuclear spin of $I = 0$ and thusly obeys Boson particle statitics at low temperatures. It undergoes a phase-transition to a superfluid at 2.177K. ^{3}He has $I = \frac{1}{2}$ and therefore obeys Fermi statistics, and it does not undergo a phase transition to a superfluid, until around 2.4mK However, as can be seen on Figure 31, the mixture of the two isotopes creates interesting features in the phase-diagram. Due to the finite solubility of ^{3}He in ^{4}He, once a sufficiently low temperature has been reached, starting at 0.87K, the mixture seperates into two phases, a normal fluid and a superfluid. The superfluid phase has a lower concentration of ^{3}He, and a higher concentration of ^{4}He, than the normal fluid, which entirely consists of ^{3}He. The heavier, dilute, superfluid phase sinks to the bottom of the container, while the lighter, concentrated, normal fluid floats on top. The difference in enthalpy of the pure ^{3}He phase and the ^{3}He-^{4}He mixture, is the driving force for the cooling of the mixture.

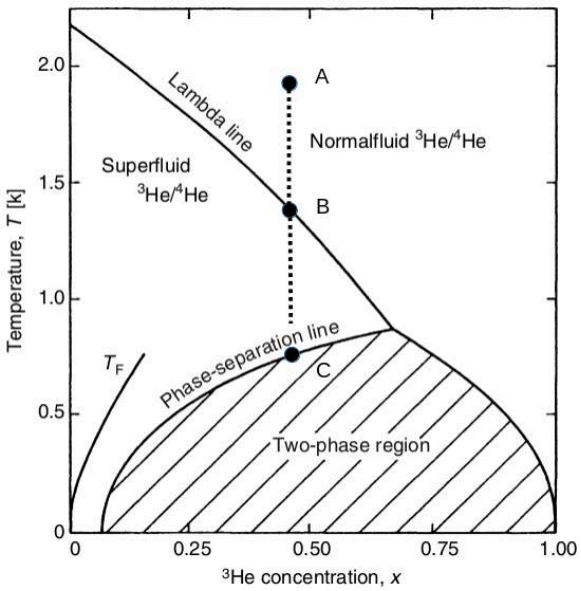

Figure 31:
Phase Diagram

Phase diagram of liquid ^{3}He- ^{4}He at saturated vapour pressure, with phase change path ABC. Adapted from[111]

By decreasing the concentration of ^{3}He in the superfluid, ^{3}He atoms will cross the phase boundary and occupy vacant energy states in the superfluid in an endothermic reaction.
This is achieved with the use of a still and heat exchange. By allowing mixture to heat up, and travel through the still, we can extract the ^{3}He atoms, which are then pumped into the mixing chamber again. For a more in-depth explanation of the dilution refrigeration technique, see F. Pobell[111].

The dilution fridge used for this experimental set-up, is the Bluefors XLD-400. The fridge is also equipped with a 6 T Tesla magnet, which is utilised for the Hall Effect measurements. All Hall effects were measured on this set-up.

4.6.2 Adiabatic Demagnetisation Refrigeration

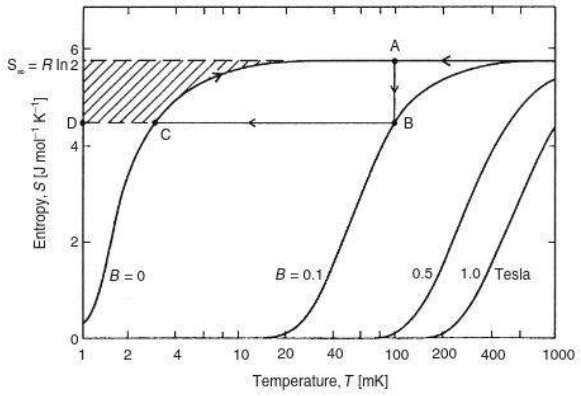

Figure 32: : Entropy Curves

Molar entropy of a single crystal of the paramagnetic salt CMN, with angular momentum $J = \frac{1}{2}$ as a function of the applied magnetic field along the crystallographic direction x[111].

Adiabatic Demagnetisation Refrigeration makes use of the relation between disordered, paramagnetic entropy, and the external applied magnetic field. As seen on Figure 32, a paramagnetic salt is first isothermally magnetised, $A \rightarrow B$, then adiabatically demagnetised, $B \rightarrow C$. From this point, the salt can then absorb heat from the sample, which moves it along the entropy curve. The heat of magnetisation during the initial process, is given by the rectangle $ABDS_{\text{inf}}$. The cooling power of the salt, after demagnetisation, is given by the shaded area $ACDS_{\text{inf}}$[111]. After the cycle is finished, it can be repeated.

While this technique is generally inferior, in terms of cooling power and continuity, to the dilution refrigeration technique, it is still a valuable tool for reaching temperatures below 1 K. The main advantage of ADR is the ability to reach temperatures around 300 mK, within a few hours of loading the sample, which is an order of magnetude faster than dilution refrigeration. This allows for a higher rate of data collection, which is important for early developement of designs.

The specific ADR system used in this work is the L-Type Rapid Kiutra, which was used for all transport measurements.

5.

Experimental Set-up and Measurements

In this section, we delve into the various techniques used in the experimental set-up, and the measurements performed in this work. We introduce the DC measurement set-up. We then move on to the transport measurements, which were performed on two different systems; a hole-transistor and a quantum dot.

There a few techniques, that were introduced in Section 2, that are not covered in this section, as fabricational issues with the device, prevented us from performing them. These techniques we were prevented from performing are namely charge sensing, RF-reflectometry, and EDSR.

5.1 DC Measurements

Various types of measurements have been performed during this work, but all of them are DC measurements. The nomenclature simply refers to the use of a DC signal, in concordance with an AC signal, to measure the current through and voltage across a sample.

In this section, we cover the experiments in which the Quantum Hall effect has been studied, and the transport measurements performed on a hole-transistor and a quantum dot.

5.1.1 Measurements of the Quantum Hall Effect

DC measurements have been performed in this work. An example schematic can be seen on Figure 33. This particular schematic showcases the Hall bar, which was used to measure the Hall effect, the theory of which was explained in Section 2.4. The target of this measurement, is to measure the voltage across probe 1 (P1) and probe 2 (P2), V_{xx}, the voltage across probe 2 (P2) and probe 3 (P3), V_{xy}, and the current, I_{SD}, as a function of the applied top gate voltage V_t and the external magnetic field, $B_\perp$.

The input voltage put on the source (S), is a mixture of a DC signal, provided by the QDAC-II, and an AC signal, provided by the SRS830 lock-in amplifier. The DC signal is the main signal, while the AC signal provides a small periodic, perturbation to the DC signal, which creates a known peak in the $\frac{1}{f}$ noise spectrum. This peak provides robustness in the measurement, as it can be demodulated by the SRS850 lock-in amplifiers, and used to calibrate the measurement. The AC perturbation from the SRS830 is connected back to the SRS860s as a reference signal, which is used to demodulate the signal.

The top gate voltage is provided by the QDAC-II, as nothing is measured from this gate, there is no need to have the fine filtering provided by the lock-in amplifiers. The external magnetic field is provided by a 6 Tesla magnet, which is part of the Bluefors XLD-400 dilution fridge.

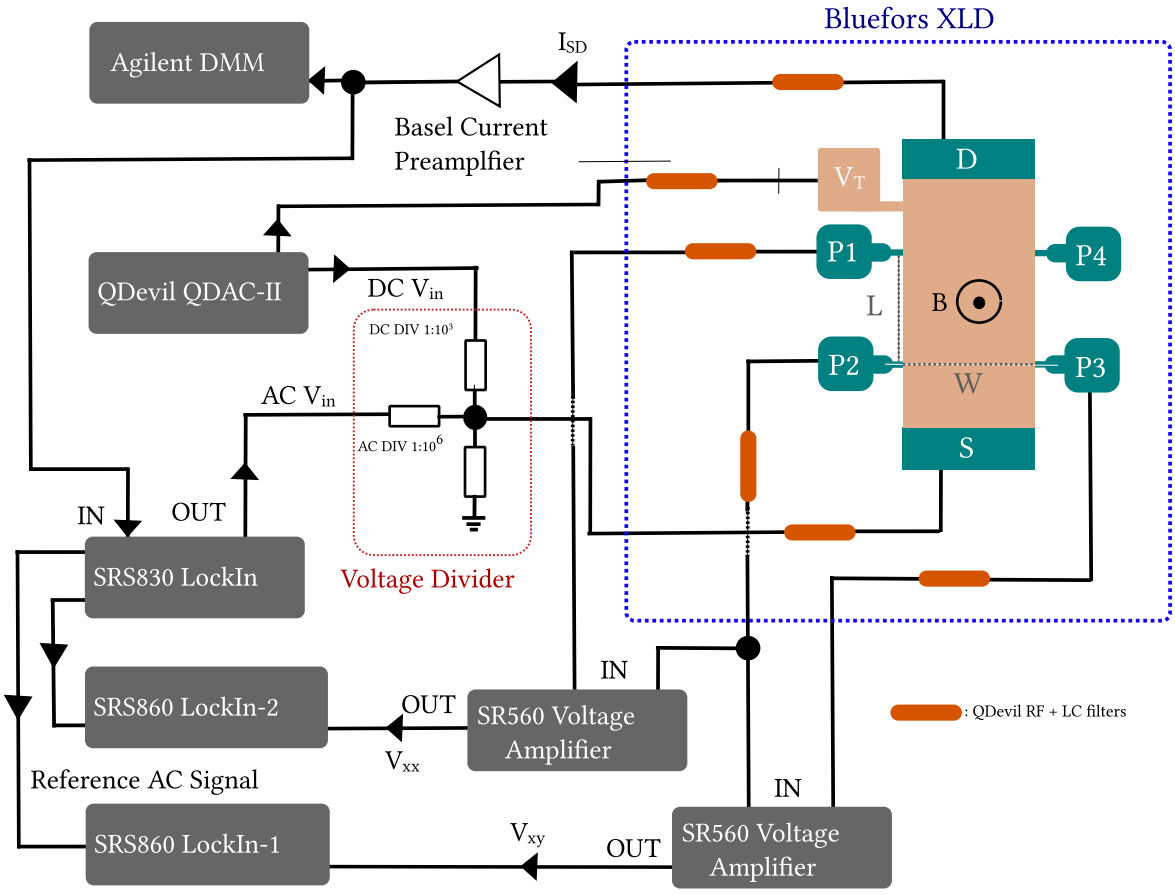

Figure 33 A schematic of the Hall bar, which was used to measure the Hall effect. The Hall bar is a 2D electron system, with a top gate voltage applied to control the carrier density. The external magnetic field is applied perpendicularly to the sample, and the Hall voltage, V_{xy}, and the longitudinal voltage, V_{xx}, are measured, along with the current I_{SD}

The output current, I_{SD}, is pre-amplified at room temperature by a Basel current amplifier, set to E^7 amplification, before being connected to the SRS830 Lock-in Amplifier and an Agilent 34465A Digital Multimeter.

The output voltages, V_{xy} and V_{xx}, are pre-amplified at room temperature by a Standford Research System SR560 Low-noise Voltage Preamplifier, set to 1000 amplification and a low-pass filtering of $100Hz$, before being connected to the SRS830 Lock-in 1 and SRS830 Lock-in 2, respectively.

As introduced in Section 2.4, the Quantum Hall effect is a quantum-mechanical phenomenon, which occurs when a 2D electron system is subjected to a strong magnetic field at low temperatures. The Hall effect is quantised, and the Hall resistivity, ρ_{xy}, shows plateaus at integer values of the filling factor, ν.

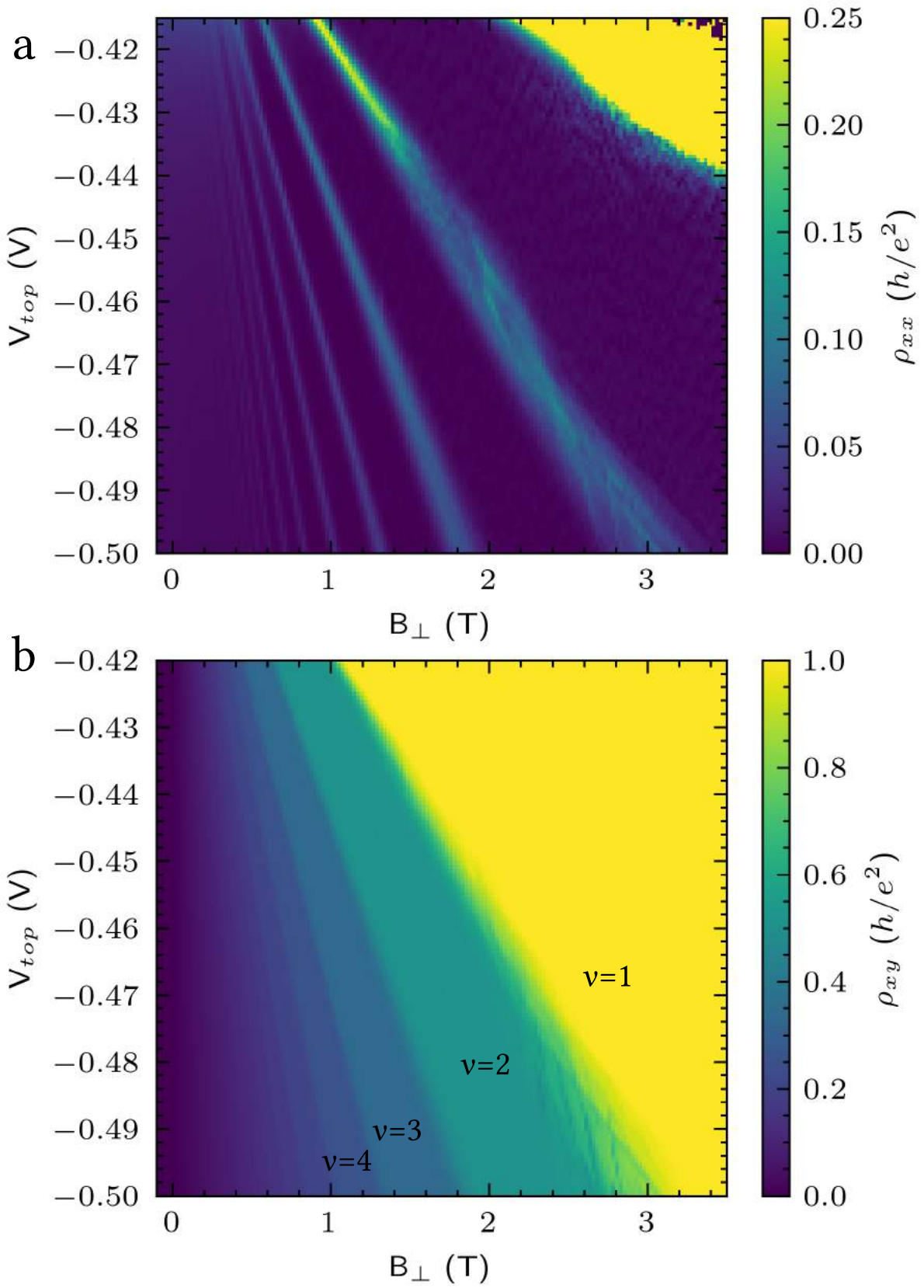

Figure 34 2-dimensional scans of the top gate voltage of the Hall bar, and the external, perpendicularly applied magnetic field. The top gate was swept in the range of [−350, −550] mV, while the magnetic field was swept from [−0.1, 6] T. **a**: The longitudinal resistivity, ρ_{xx}. **b**: The Hall resistivity ρ_{xy}.

Figure 34 show Landau fans[61] with defined edges and limited broadening, with the filling factor shown in selected sections of the fan in **b**.

Figure 35, **a**, is a line-cut at the white dashed line seen on Figure 34, at a top gate value of −490.4 mV and as can be seen plateaus are distributed around integer values of ν, while their values vary from their particular integer by $2 - 2.8\%$.

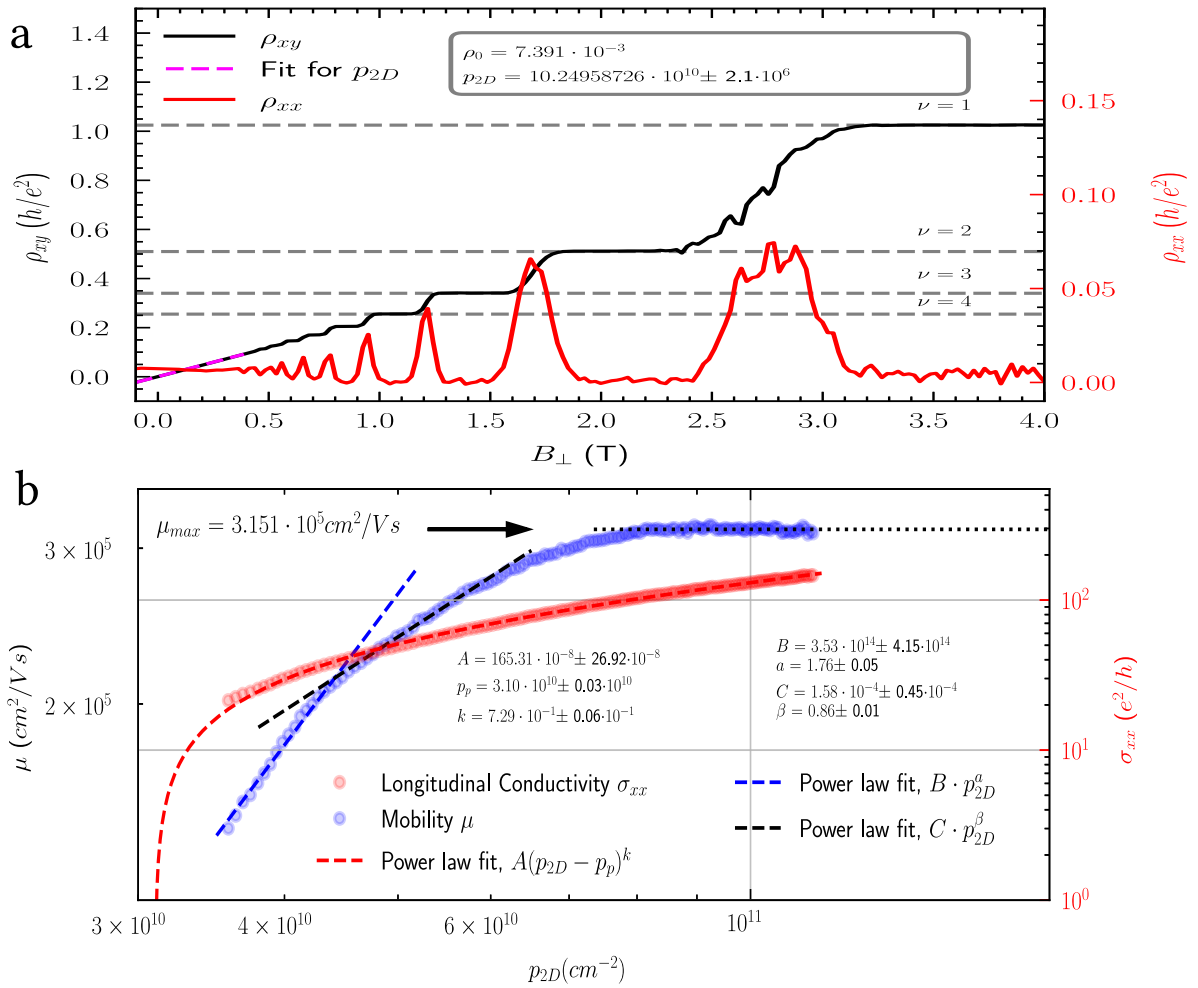

Figure 35 **a**: The longitudinal resistivity, ρ_{xx}, and the Hall resistivity, ρ_{xy}, as a function of the magnetic field, B, at a fixed temperature, $T = 13$ mK, in units of conductance quanta. The Hall resistivity shows plateaus at integer values of the filling factor, ν, while the longitudinal resistivity shows oscillations. The active carrier density was calculated from a fit of the linear regime of the Hall resistivity. ρ_0 was extracted from ρ_{xx} at 0 magnetic field.**b**: The mobility and conductivity, μ and σ_{xx}, respectively, given as a function of the active carrier density, p_{2D}. The average value at transport saturation is observed to be $\mu_{max} = 3.151 \cdot 10^5 \frac{cm^2}{Vs}$. A power law fit according to percolation density has been added, and from this the percolation density is calculated to be $p_p = 3.10 \cdot 10^{10} \pm 0.03 \cdot 10^{10}$ cm^{-2}. Two power law fits for the two, seperate unsaturated regions of the mobility are also seen. **Note**: They artifically extend beyond their fitting regime, to increase visibility.

A turn-on value of $V_{tc} = -399.8$ mV was observed, so to calculate the conductivity and mobility of the material, a line-cut was taken in the range of [V_{tc}, −500 mV], where p_{2D} and ρ_0 have been extracted from each. This calculation provides a specific value of p_{2D} and ρ_0 for each particular value of the top

gate voltage. Figure 35, **b**, showcases the mobility and conductivity as a function of the active carrier density.

While the scaling factor of the power law fit, A, has a significant standard deviation of $\pm 16\%$, p_p and k are both well constrained, falling around $\pm 1\%$ each.

The values of $\mu_{max} = 3.151 \cdot 10^5 \frac{cm^2}{Vs}$ and $p_p = 3.10 \cdot 10^{10} cm^{-2}$ correspond well with previous litterature[54,55,61,112] on the subject, which have reported values of $\mu_{max} = 5 \cdot 10^5 \frac{cm^2}{Vs}$ and $p_p = 1.15 \cdot 10^{11} cm^{-2}$, respectively. The power law fit of the form $\mu_{fit} = B \cdot p_{2D}^a$, in the first unsaturated region ($3.5^{10} < p_{2D} < 4.5^{10}$), yields an exponent of approximately $a = 1.76$, where $a \geq 1.5 \pm 0.05$ is an indication that the mobility is limited by scattering from strain distributions of threading dislocations[61,113,114,115]. A second fit of the same type, in the second unsaturated region, $4.5^{10} < p_{2D} < 6^{10}$ yields an exponent of $\beta = 0.86 \pm 0.01$, suggesting that this region of the mobility is primarily limited by a uniform distribution of background charges[114,113].

5.2 Transport Measurements

Transport measurement are the measurement of a current, I_{SD}, via hole charge-carriers in the 2-DHG, as a function of the top gate voltage, V_T, and the bias voltage, V_{SD}, between the source and the drain. The transport measurements were performed on two different systems; a hole-transistor and a quantum dot. The hole-transistor is a test-device, with a single top gate, and two connected ohmics (See Figure 36). The quantum dot is a sensor-dot configuration, with a plunger gate, two barrier gates, a screening gate, and two connected ohmics (See Figure 39).

5.2.1 Hole Transistor

The first transport measurements were performed on a hole-transistor, which is a test-device, with a single top gate, and two connected ohmics, shown on Figure 36.

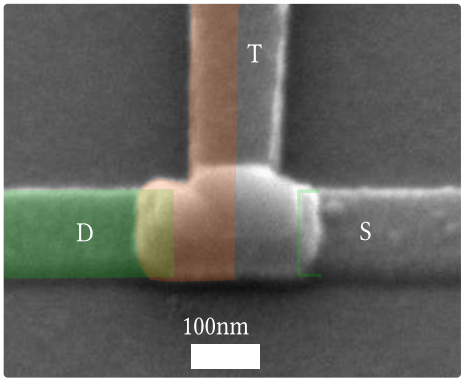

Figure 36:
Hole Transistor

Half-false-coloured hole transistor with a single top gate (T), and two connected ohmics (S and D). Ohmic: Green. Red: Plunger

All gates were connected to the QDAC-II, which controlled both the voltage input and measured the current output.

Figure 37, **a**, shows a clean turn-on of the transistor, with $V_{SD} = -2$ mV, and a symmetric I_S and I_D, as a function of the top gate voltage, V_T. The average difference in current, $\overline{\Delta I}$, between the two currents is low, and the current is linear with the top gate voltage. By a applying a linear fit which follows: $R_{ch} = \frac{\Delta V}{\Delta I}$, the channel resistance, R_{ch}, was calculated to be 13.38 kΩ, seen on Figure 37, **b**.

However, as the device stays on, I_{SD} will drift towards zero. This is due to Fowler-Nordheim tunneling, which occurs between the 2-DHG and the surface interface.[116,117]
Figure 38 shows a sketch of the valence energy band in the Ge/SiGe heterostructre, as a function of depth. There is an initial hole density, populated by accumulation, located at approximately 55 nm into the heterostructure, which is the depth of the Ge layer.

As the device remains on, tunneling will occur between the 2-DHG and the surface interface, causing holes to be trapped in the various surface defects and impurities, effectively creating a screening layer of charges below the top gate. This screening layer will reduce the electric field in the 2-DHG, which

will reduce the current, I_{SD}, and the device will turn off. This is known as hysteric drift and it occurs due to the Fowler-Nordheim tunneling.

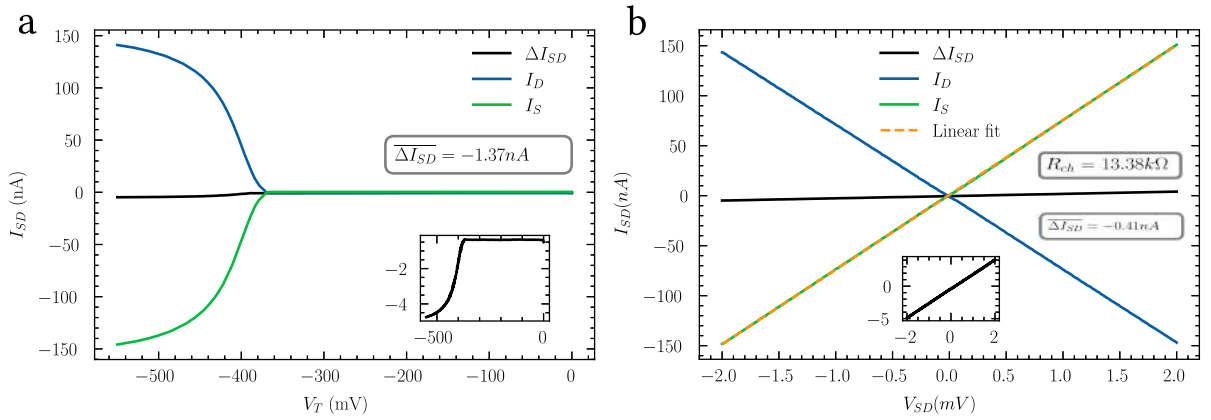

Figure 37 **a**: The current, measured at the source and the drain, as a function of the top gate voltage, V_T, with the average difference in current, $\overline{\Delta I_{SD}}$, between the two currents shown. Insert: Shows the difference in current, ΔI_{SD}. **b**: The current, measured at the source and the drain, as a function of the bias voltage between the source and the drain, V_{SD}. Also shown is a linear fit to source current. The channel resistance, R_{ch}, was calculated to be 13.38 kΩ. Insert: Shows the difference in current, ΔI_{SD}

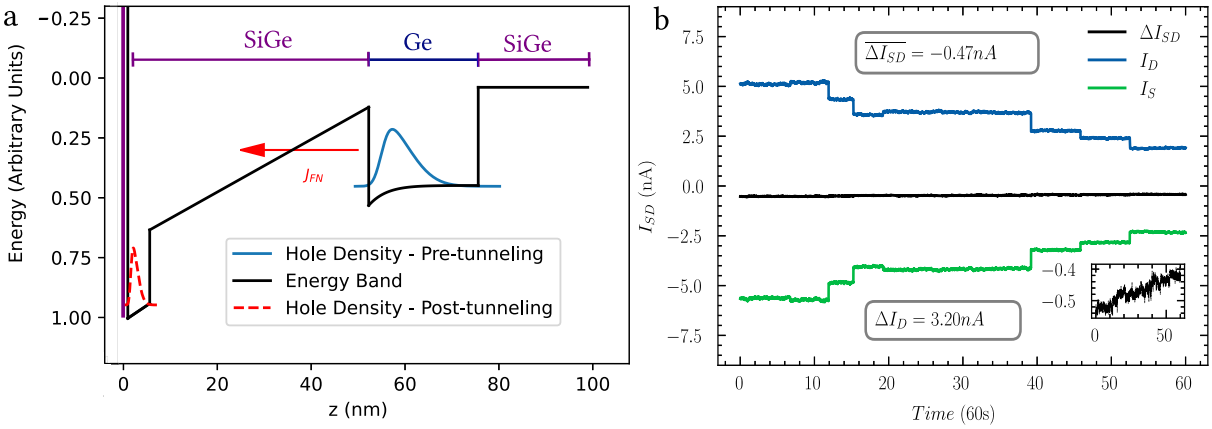

Figure 38 **a**: Sketch illustration of Fowler-Nordheim tunneling. The initial hole density, blue, and an additional hole density following tunneling, dashed-red, are shown. The Fowler-Nordheim current, J_{FN} is indicated with a red arrow. Adapted from[116]. **b**: I_{SD} as a function of time, where the current drifts towards zero. The source-drain current, ΔI_{SD} difference, the average source-drain current difference , $\overline{\Delta I_{SD}}$, as well as the head-to-tail difference in drain current ΔI_D is shown. Insert: Shows the different in current, ΔI_{SD}

Investigating the drift in the I_{SD} by parking the top gate voltage at −380 mV and setting the bias voltage $V_{SD} = -2$ mV, and measuring the currents, I_D and I_S, as a function of time,

Figure 38, **b**, shows a significant drift in the current, I_{SD}, towards zero, as tunneling occurs between the 2-DHG and the surface interface.

$\overline{\Delta I_{SD}}$ remains low, indicating isolated gates, where no leakage occurs. The head-to-tail difference in drain current, ΔI_D, is observed to be 3.20 nA, amounting to a 63.3% decrease.

5.2.2 Quantum Dot Measurements

The sensor dot configuration can be seen on Figure 39, and an SEM image of it can be seen on Figure 19, **d**. For these experiments, the ohmic contacts designated as O1B acted as the source, and O1T acted as the drain. The screening (or cut-off) gate, SS2, was off for all following measurements. The pinch-off barriers, SP1BB, SP1BT, and the sensor plunger, SP1 were initially used as a cluster, and are designated as Left Sensor Plunger Cluster (LSPC).

All gates were connected to the QDAC-II, and which controlled both the voltage input and measured the current output.

As can be seen on Figure 40, **a**, the sensor dot turned on, meaning there is current flow between the source and drain, while sweeping the LSPC. The currents are approximately symmetric and equal, as evidented by the low average difference in current, $\overline{\Delta I}$. While there is a tendency for $\overline{\Delta I}$ to follow the source current, it is a factor of 50 smaller than the measured current. It is therefore interpreted as an artifact of the measurement equipment.

Figure 40, **b**, shows the current as a function of the bias voltage between the source and the drain. The current is symmetric around zero, and linear with the bias voltage, which is a sign that no leakage occurs in the system, indicating that all gates are electrically isolated and the isolating dielectric is intact. The channel resistance was calculated to be: $R_{ch} = 41.27$ kΩ.

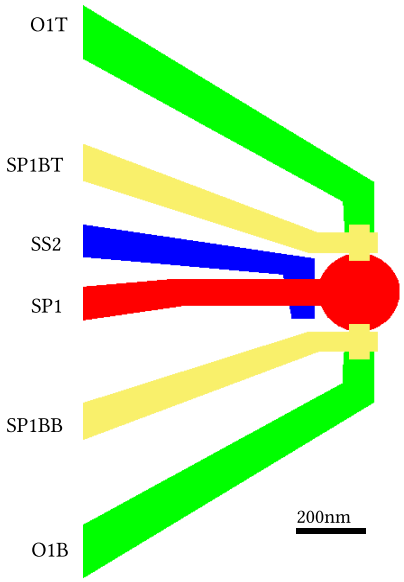

Figure 39: Sensordot Configuration

Quantum dot configuration. Ohmic leads: orange, starting code O1. Pinch-off barriers: blue, starting code SP1B. Quantum dot: burgundy, code SP1. Screening gate: purple, code SS2.

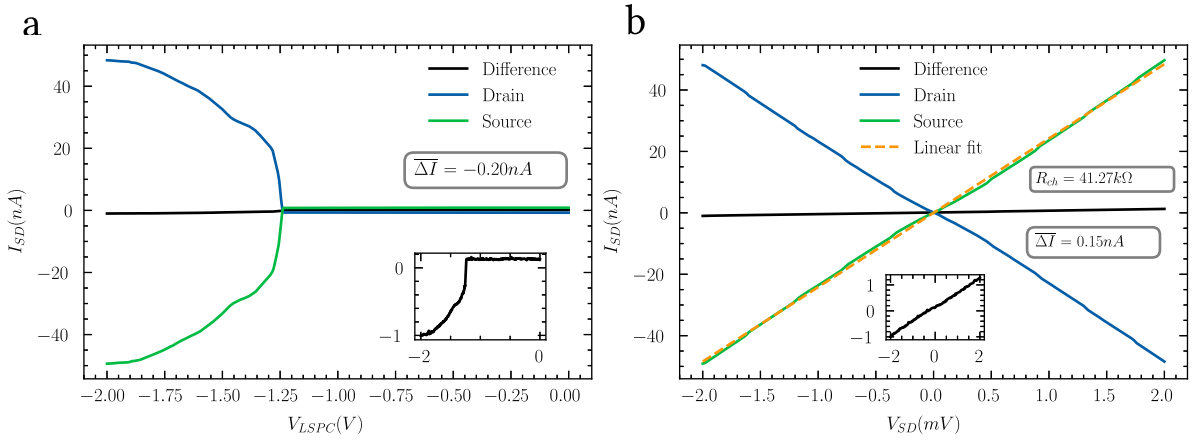

Figure 40 **a**: The current, measured at the source and the drain, as a function of the LSPC voltage, V_{LSPC}, with the average difference in current, $\overline{\Delta I}$, between the two currents shown. **b**: The current, measured at the source and the drain, as a function of the bias voltage between the source and the drain, V_{SD}. Also shown is a linear fit to source current. The channel resistance, R_{ch}, was calculated to be 41.27 kΩ.

As the sensor can turn on with the cluster, it is vital to investigate the pinch-off barriers and the sensor plunger individually, as their individual functionality is vital for a functioning sensor dot. This is done by parking the whole cluster at a turned on voltage, and then sweeping the voltage on each individual gate, while measuring the current between the source and the drain. Initially, the voltage is swept to

the pinch-off region, i.e., values closer to 0 V. Then it is swept back into a higher numerical value. The turn-on and pinch-off curves for each gate in the cluster, can be seen on Figure 41.

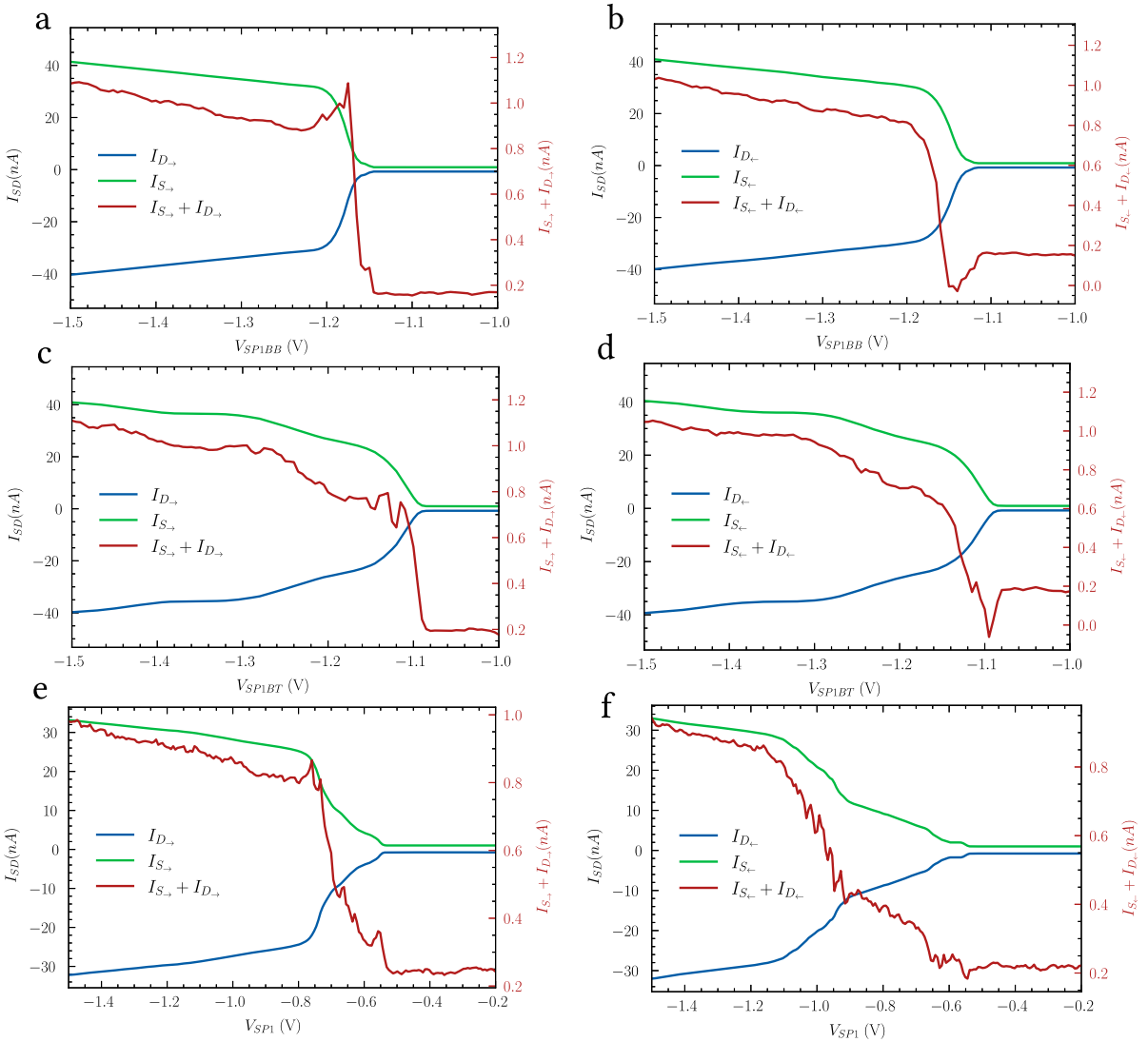

Figure 41 **a**, **b**: Turn-on and pinch-off curves for the bottom pinch-off barrier, respectively. **c**, **d**: Turn-on and pinch-off curves for the top pinch-off barrier, respectively. **e**, **f**: Turn-on and pinch-off curves for the sensor plunger, respectively. All are plotted with the difference in current, ΔI, between the source and the drain.

All three gates in the cluster showcase excellent ability to both turn on the current and pinch it off. However, the turn-on value and the pinch-off value vary slightly, depending on the direction that is being swept. This is due to the hysteresis in the system, which is a common feature in these types of measurements.

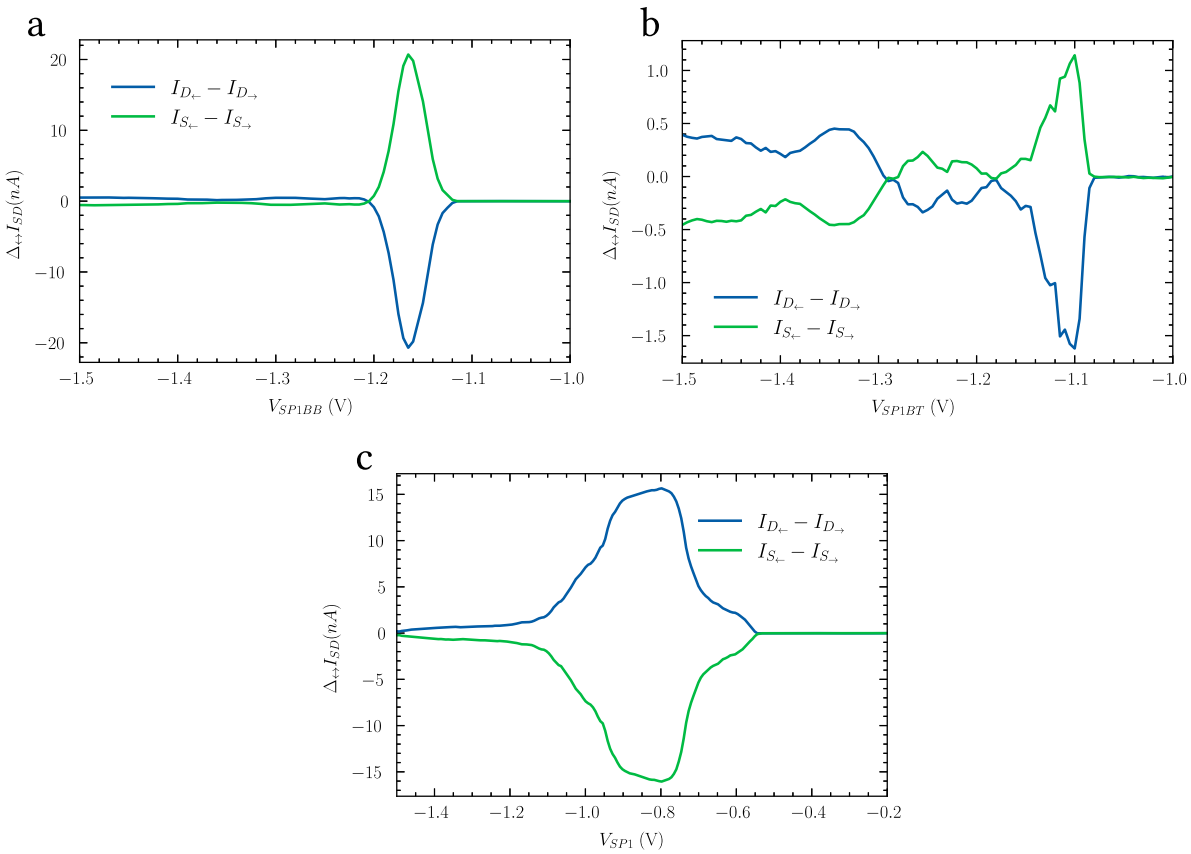

Figure 42 **a**: Hysteresis in the system from bottom pinch-off barrier. **b**: Hysteresis in the system from top pinch-off barrier. **c**: Hysteresis in the system from sensor plunger.

Figure 42 shows the hysteresis in the system, as a function of the voltage on the gates. The hysteresis is a result of the Fowler-Nordheim drift mentioned in Section 5.2.1, and is a common feature in these types of measurements.

As expected from previous work[118,119,120], the largest variation in $\Delta_\leftrightarrow I_{SD}$ is seen during turn-on/pinch-off, as this is where the hysteresis would have the largest effect. Especially Figure 42, **a**, showcase a particularly large hysteresis around turn-on/pinch-off, that otherwise approaches zero. Figure 42, **b**, and **c**, show a similar trend.

Succesfully having demonstrated pinch-off using all gates in the cluster, the next step is to investigate the lowest value for both pinch-off barriers at which the transistor is still on, such that the sensor plunger has the largest effect on the system.

Figure 43, **a**, shows a two-dimensional scan, sweeping both the bottom and top pinch-off barriers, V_{SP1BB} and V_{SP1BT}, while measuring the current between the source and the drain, I_{SD}. The pinch-off values for the two gates are approximately symmetric, centered around –1.2 V. Parking both

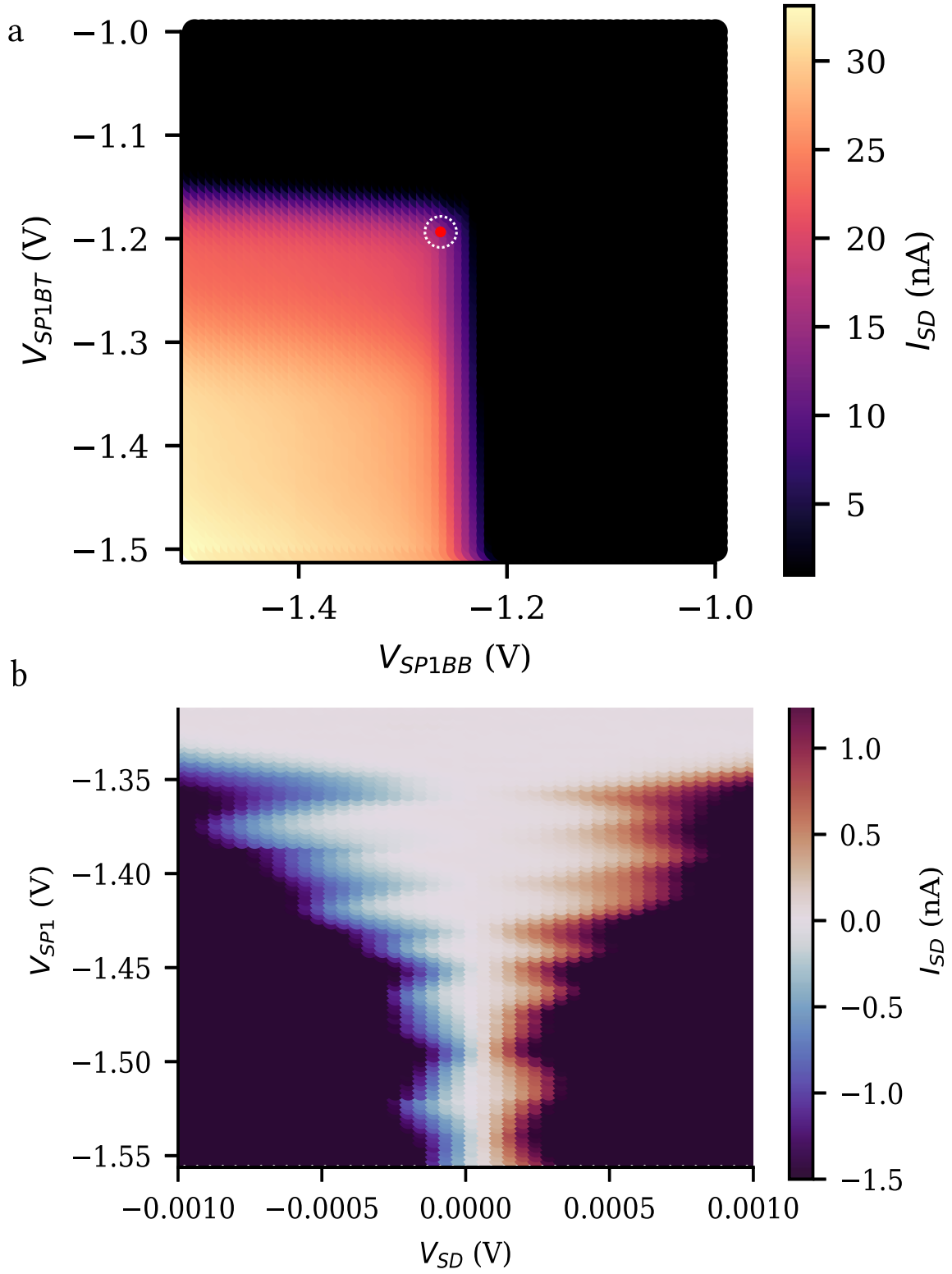

Figure 43 **a**: A two-dimensional scan, sweeping V_{SP1BB} and V_{SP1BT}, while measuring the current between the source and the drain, I_{SD}. Bias spectroscopy parking spot indicated with a bull's eye. **b**: Bias spectroscopy; sweeping the bias voltage, V_{SD} and the plunger gate voltage, V_{SP1}, while measuring, I_{SD}.

pinch-off barriers at the bull's eye indicated on Figure 43, **a**,, the sensor plunger, SP1, and the voltage bias, V_{SD}, are swept, while measuring the I_{SD}. This experiment is called bias spectroscopy and is shown on Figure 43, **b**. The bias spectroscopy is used to investigate the charging energy of the sensor dot, and to find the optimal working point for the sensor dot. The resolution of this scan is low, and time did not permit for further tuning of the dot, so well-defined Coulomb diamonds are not visible, however, there is a trend reminiscent of Coulomb diamonds.

Had time allowed, a more suitable area of decoupling from the barrier gates would have been found, and the sensor plunger would have been tuned to a more optimal working point. Following this, instead of DC measurements, a lock-in amplifier, such as the one utilised in Section 5.1.1, would have been connected, as it allows for a far more sensitive scan.

6.

Conclusion and Outlook

We conclude our work with a summation, conclusion, and outlook.
In the thesis work we have designed, simulated, fabricated, and measured three-layer, nano-scale devices, laying the ground-work for further work on scalable 2×N devices. The design and simulation process has been automated, such that design features can be changed by a single change of parameter, and no further work is needed, to make it compatible with the simulation platform, Section 2.5.1. The simulatatory work has been shown to be stable, convergent, and efficient for all reasonable gate voltage ranges, and that it provides a realistic representation of the static electric fields, Section 3. We have shown that the devices can be fabricated using the techniques outlined in this work. Of said fabrication, we solved numerous issues such namely the incompatibility of previous fabricational recipes with the need for aluminium ohmics, and the fine-tuning of the Al_2O_3 between layers, such that a workable lever-arm is present, without incurring leakage between gates, Section 4. We have performed DC measurements, to measure functional hole-transistors, which were used to demonstrate heterostructure-specific physics in the form of hysteric drift. We have characterised the system by employing the Hall effect, to investigate the mobility and conductivity of the 2-DHG in the substrate. Lastly, a sensor dot was turned on, which was shown to be sensitive to the presence of single holes via bias spectroscopy, Section 5.
There is still a long way to go, for a full 2x2 or 2x3 array to be functional. We would need to demonstrate single hole-occupancy, perform RF-reflectrometry and charge-conversion charge sensing, and most importantly, tune and operate spin qubits. This is a long and arduous process, now outside the scope of this thesis, but we believe that the work done in this thesis is a solid foundation for such further work.

6.1 Outlook

The immediate next step would be to tune the sensor dot into a single-hole regime, and perform RF-reflectrometry on it. This would allow us to demonstrate single-hole occupancy, and would be a necessary step for sanity-checking and further developement of the design. Following that, the next step would be to fabricate a 2x2 or 2x3 array, and demonstrate charge sensing in a double quantum dot, as this is the simplest, coupled system we can measure. Lastly, the spin qubits would need to be tuned and operated, and the system would need to be characterised in terms of coherence times and fidelity. This would be the final step in the process of demonstrating the feasibility of this design, and would be the most challenging.
Besides demonstrating real-world control of the design, an automated design process such as a predictor-corrector scheme coupled with machine learning, would be beneficial for further work. This would allow for rapid prototyping of new designs, and would allow for the design of more complex systems.

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7.

Appendix

In this appendix, we provide additional information that is relevant to the main body of the thesis. This includes the fabrication protocol, recipes for the various resists used in the fabrication process, and the simulation code used in the thesis. It also includes extra figures and tables that are relevant to the main body of the thesis.

7.1 Fabrication protocol - Recipes

The recipes listed in this appendix are in the order, in which they are used in the fabrication process.

7.1.1 Markers

1. Standard cleaning process for a bare chip: 10 minutes in acetone, 2 minutes of sonication, at 30 power and 80kHz frequency (gentlest setting), 5 minutes in isopropanol (IPA). Followed by drying with nitrogen gun.
2. Ash for 2 minutes in plasma asher, in O_2 atmosphere.
3. Bake for 2 minutes on a hot-plate at 115 ℃.
4. Spin-coat with CSAR13 at 4000RPM for 60 seconds.
5. Bake for 2 ½ minutes on a hot-plate at 185 ℃.
6. Exposure on Elionix 125kV tool: 1nA beam current, 500 $\frac{\mu C}{cm^2}$ dosage, 120 μm aperture, 500 μm write field size, 200000 dots, 0.88 pitch, 2.2nm pixel and beam spot size.
7. Develop in O-Xylene for 45 seconds, followed by a 30 seconds wash in IPA.
8. Ash for 2 minutes in plasma asher, in O_2 atmosphere. Optical inspection: If results are looking poor, strip in 1,3-Dioxilane and repeat from step 1.
9. Deposition of 5nm of Ti and 50nm of Au in the AJA-1 or AJA-2 e-beam evaporator.
10. Lift-off in room-temperature 1,3-Dioxilane for 2 hours. “Blow” on the chip with a pipette filled with 1,3-Dioxilane to remove any remaining resist. Sonicate in 1,3-Dioxilane for 2 minutes, at 30 power and 80kHz frequency. Transfer to glass lense for optical inspection. If poor results, repeat “blowing” and sonication, until desired results.
11. Ash in plasma asher for 2 minutes, in O_2 atmosphere.

7.1.2 Ohmics

1. Soak in Acetone for 5 minutes, followed by a 2 minute sonication at 30 power and 80kHz frequency. Wash in IPA for 2 minutes. Dry with nitrogen gun.
2. Ash for 2 minutes in plasma asher, in O_2 atmosphere.
3. Bake for 2 minutes on a hot-plate at 115 ℃.
4. Spin-coat with PMMA A4 at 4000RPM for 60 seconds.
5. Bake for 2 minutes at 185 ℃.
6. Exposure on Elionix 125kV tool:
    - Inner structures: 500pA beam current, 700 $\frac{\mu C}{cm^2}$ dosage, 120 μm aperture, 500 μm write field size, 1000000 dots, 4 pitch, 2nm pixel and beam spot size.

- Outer structures: 20nA beam current, 1100 $\frac{\mu C}{cm^2}$ dosage, 240 μm aperture, 500 μm write field size, 50000 dots, 2.2 pitch, 22nm pixel and beam spot size.

7. Develop in MIBK:IPA 1:3 for 60 seconds, followed by a 15 second wash in IPA. Dry with nitrogen gun.
8. Pre-bake on hot-plate for 20 seconds at 100 ℃.
9. Dip in 6% buffered hydroflouric acid solution for 10 seconds, followed by three seperate 10-second washes in millipore water, followed by a 10 second wash in IPA. Dry with nitrogen gun. Quick optical inspection. If the HF etch has caused resist-delamination, strip in acetone and repeat from step 1.
10. Rush into AJA-1 or AJA-2 e-gun evaporator for deposition of 22nm of Al.
11. Lift-off in room-temperature 1,3-Dioxilane for 2 hours. "Blow" on the chip with a pipette filled with 1,3-Dioxilane to remove any remaining resist. Sonicate in acetone for 2 minutes, at 30 power and 80kHz frequency. Transfer to glass lense for optical inspection. If poor results, repeat "blowing" and sonication, until desired results.

7.1.3 Atomic Layer Deposition

1. Pre-bake ALD chamber at 150 ℃ for 2 hours, to clear possible contaminants.
2. Ash for 2 minutes in plasma asher, in O_2 atmosphere.
3. Place chip in ALD chamber, at site A, as mentioned in Section 4.5.6, with dummy chip on site B.
4. Bake chamber at 250 ℃ for 2 ½ hours.
5. Reduce chamber temperature to 150 ℃ and start ALD procedure. 75 cycles total, should yield approximately 7nm of Al_3O_2. The cycle parameters are:
   - Trimethylaluminium:
     - Pulse time: 0.02 seconds
     - Purge time: 20 seconds
   - H_2O:
     - Pulse time: 0.5 seconds
     - Purge time: 20 seconds

7.1.4 Silicone-Dioxide Protection Ridge

1. Soak in Acetone for 5 minutes, followed by a 2 minute sonication at 30 power and 80kHz frequency. Wash in IPA for 2 minutes. Dry with nitrogen gun.
2. Ash for 2 minutes in plasma asher, in O_2 atmosphere.
3. Bake for 2 minutes on a hot-plate at 115 ℃.
4. Spin-coat with PMMA EL9 co-developer at 4000RPM for 60 seconds.
5. Bake for 2 minutes at 185 ℃.
6. Spin-coat with PMMA EL9 co-developer at 4000RPM for 60 seconds.
7. Bake for 2 minutes at 185 ℃.
8. Spin-coat with PMMA A4 at 4000RPM for 60 seconds.
9. Bake for 2 minutes at 185 ℃.
10. Exposure on Elionix 125kV tool: 20nA beam current, 1300 $\frac{\mu C}{cm^2}$ dosage, 240 μm aperture, 500 μm write field size, 50000 dots, 2.2 pitch, 22nm pixel and beam spot size.
11. Develop in MIBK:IPA 1:3 for 60 seconds, followed by a 30 seconds wash in IPA.
12. Ash for 2 minutes in plasma asher, in O_2 atmosphere.
13. Deposition of 180nm SiO_2 in the Kurt J. Lesker e-gun evaporator.
14. Lift-off in 50 ℃ acetone for 2 hours. "Blow" on the chip with a pipette filled with acetone to remove any remaining resist. Sonicate in acetone for 2 minutes, at 30 power and 80kHz frequency. Transfer to glass lense for optical inspection. If poor results, repeat "blowing" and sonication, until desired results.

7.1.5 Top gates

1. Soak in Acetone for 5 minutes, followed by a 2 minute sonication at 30 power and 80kHz frequency. Wash in IPA for 2 minutes. Dry with nitrogen gun.
2. Ash for 2 minutes in plasma asher, in O_2 atmosphere.
3. Bake for 2 minutes on a hot-plate at 115 ℃.
4. Spin-coat with CSAR4 at 4000RPM for 60 seconds.
5. Bake for 2 minutes at 185 ℃.
6. Exposure on Elionix 125kV tool:
    - Inner structures: 500pA beam current, 200 $\frac{\mu C}{cm^2}$ dosage, 120 μm aperture, 500 μm write field size, 1000000 dots, 4 pitch, 2nm pixel and beam spot size.
    - Outer structures: 20nA beam current, 400 $\frac{\mu C}{cm^2}$ dosage, 240 μm aperture, 500 μm write field size, 50000 dots, 2.2 pitch, 22nm pixel and beam spot size.
7. Develop in O-Xylene for 45 seconds, followed by a 30 second wash in IPA. Dry with nitrogen gun.
8. Ash for 2 minutes in plasma asher, in O_2 atmosphere.
9. Deposition of 5nm Ti followed by 22nm of Pd in the AJA-2 e-beam evaporator.
10. Lift-off in room-temperature 1,3-Dioxilane for 2 hours. “Blow” on the chip with a pipette filled with 1,3-Dioxilane to remove any remaining resist. Sonicate in 1,3-Dioxilane for 2 minutes, at 30 power and 80kHz frequency. Transfer to glass lense for optical inspection. If poor results, repeat “blowing” and sonication, until desired results.
11. Repeat Section 7.1.3
12. Repeat steps 1-10, with a deposition of 28nm of Pd instead.
13. Repeat Section 7.1.3
14. Repeat steps 1-10, with a deposition of 34nm of Pd instead.

7.1.6 Buffer Stacks

1. Soak in Acetone for 5 minutes, followed by a 2 minute sonication at 30 power and 80kHz frequency. Wash in IPA for 2 minutes. Dry with nitrogen gun.
2. Ash for 2 minutes in plasma asher, in O_2 atmosphere.
3. Bake for 2 minutes on a hot-plate at 115 ℃.
4. Spin-coat with CSAR13 at 4000RPM for 60 seconds.
5. Bake for 30 seconds on a hot-plate at 150 ℃.
6. Spin-coat with CSAR13 at 4000RPM for 60 seconds.
7. Bake for 60 seconds on a hot-plate at 150 ℃.
8. Exposure on Elionix 125kV tool: 20nA beam current, 500 $\frac{\mu C}{cm^2}$ dosage, 240 μm aperture, 500 μm write field size, 50000 dots, 2.2 pitch, 22nm pixel and beam spot size.
9. Develop in O-Xylene for 60 seconds, followed by a 30 seconds wash in IPA.
10. Transene-D etch for 130 seconds in 50 ℃ Transene-D. Followed by 10 seconds wash in 50 ℃ millipore bath, followed by 10 second wash in room-temperature millipore bath.
11. Strip in 1,3-Dioxilane for 1 hour. “Blow” on the chip with a pipette filled with 1,3-Dioxilane to remove any remaining resist. Sonicate in 1,3-Dioxilane for 2 minutes, at 30 power and 80kHz frequency.
12. Repeat steps 1-9.
13. Ash in plasma asher for 2 minutes, in O_2 atmosphere.
14. Deposition of 50nm of Ti, 100nm Al, 50nm Ti, 50nm Al in the AJA-1 or AJA-2 e-beam evaporator.
15. Lift-off in room-temperature 1,3-Dioxilane for 2 hours. “Blow” on the chip with a pipette filled with 1,3-Dioxilane to remove any remaining resist. Sonicate in 1,3-Dioxilane for 2 minutes, at

30 power and 80kHz frequency. Transfer to glass lense for optical inspection. If poor results, repeat “blowing” and sonication, until desired results.

7.2 Complimentary Figures

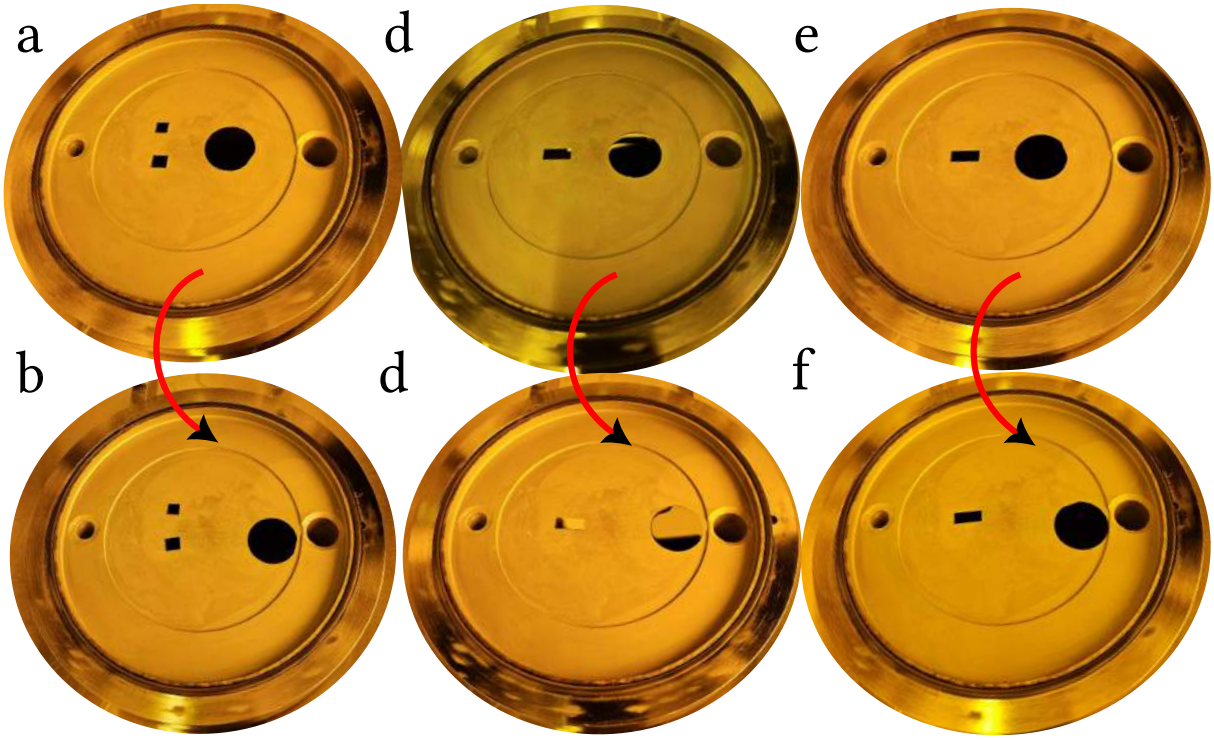

Figure 44 Optical images showcasing the displacement of the chip and dummy chip in the ALD chamber, for three out of the nine runs, used in the data analysis. The chip is placed at site A, while the dummy chip is placed at site B. **a**: Initial placement for run a. **b**: Final displacement run a. **c**: Initial placement for run b. **d**: Final displacement run b. **e**: Initial placement for run c. **f**: Final displacement run c.

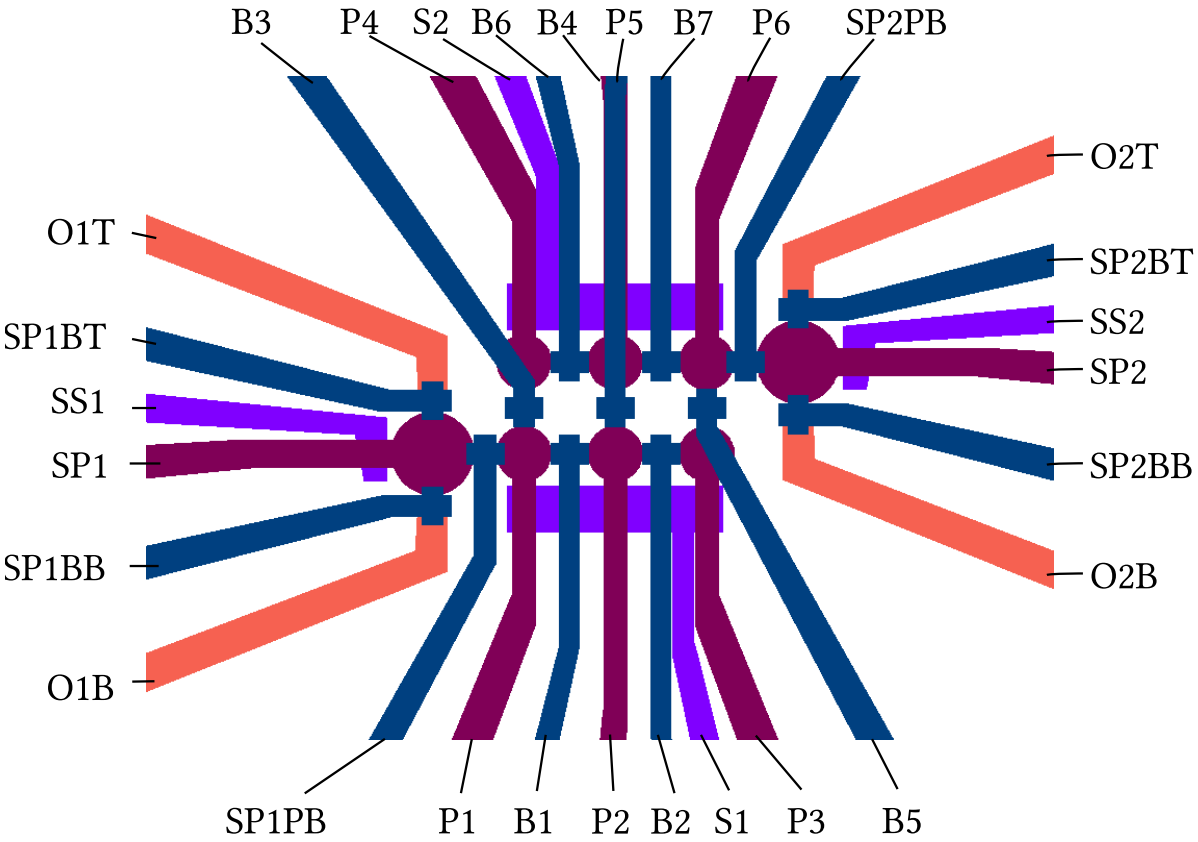

Figure 45 The alpha-numerical codes used for the leakage matrix diagnostics in Section 4.2.4.

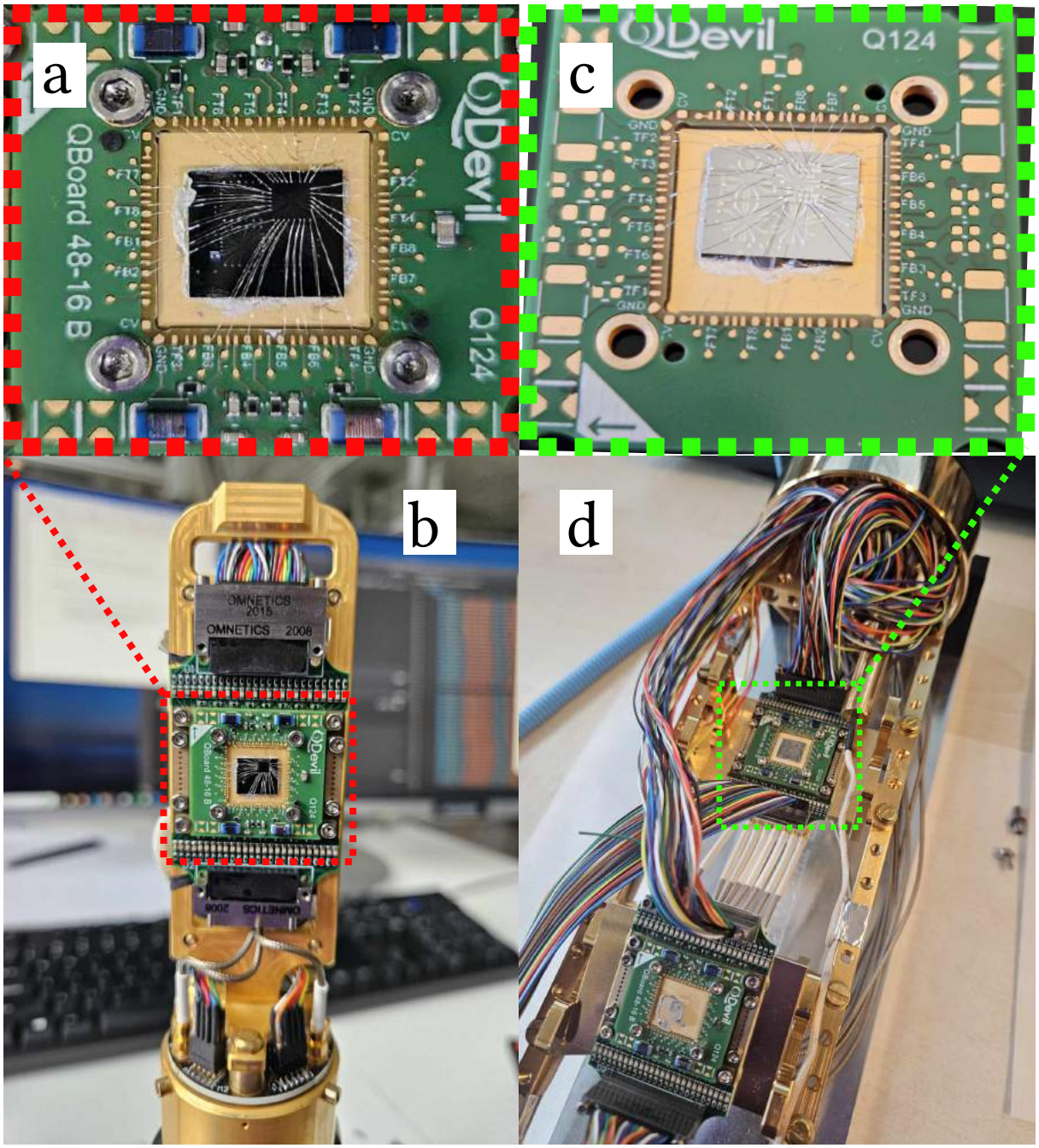

Figure 46 **a**: Close-up of the AXL MkVII chip, where the top 2x3 quantum dot array device has been bonded. **b**: Above mentioned chip loaded into the Kiutra puck, right before cool-down. **c**: Close-up of the AXL MkX chip, where the full test-structure in the bottom corner has been bonded. **d**: Above mentioned chip loaded into the Bluefors puck, right before cool-down.

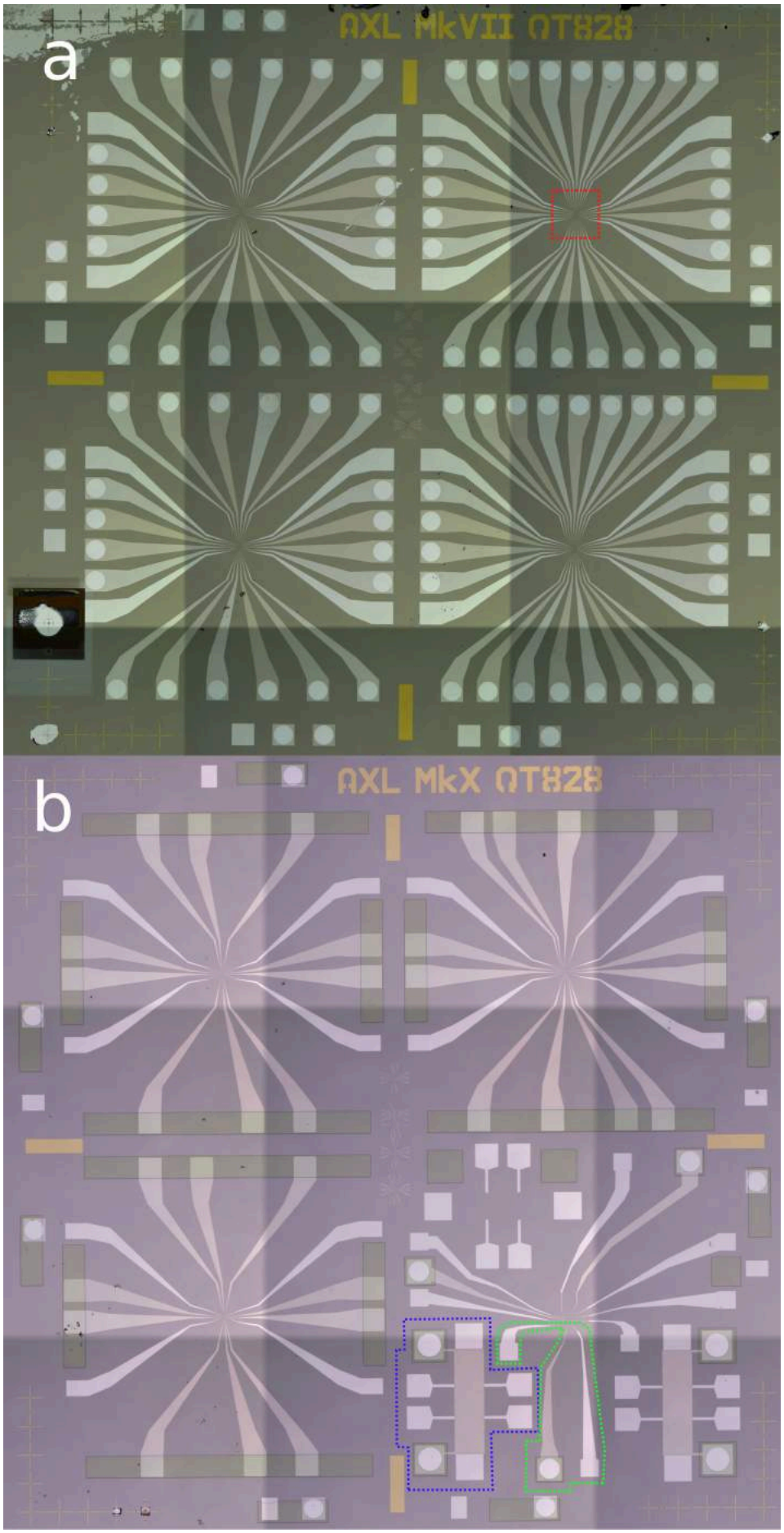
a
AXL MkVII QT828
b
AXL MkX QT828

Figure 47 **a**: Full AXL MkVII chip. Highlighted in a red outline, is the device used for transport measurements in a quantum dot (See Section 5.2.2). **b**: Full AXL MkX chip. Highlighted in a green outline is the hole-transistor used for transistor and transport measurements (See Section 5.2.1). Highlighted in a blue outline is the Hall bar used for quantum Hall effect measurements (See Section 5.1.1).